WEST

End of Result Set

☐ Generate Collection

L2: Entry 1 of 1 File: JPAB Jan 12, 1999

PUB-NO: JP411008330A
DOCUMENT-IDENTIFIER: JP 11008330 A
TITLE: MANUFACTURE OF SEMICONDUCTOR PACKAGE

PUBN-DATE: January 12, 1999

INVENTOR-INFORMATION:

NAME	COUNTRY
ISHIDA, YOSHIHIRO	
SHIMIZU, KIYOSHI	
SATO, TETSUO	
NISHIKATA, SHINICHI	
OHARA, TSUTOMU	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
CITIZEN WATCH CO LTD	

APPL-NO: JP09158689
APPL-DATE: June 16, 1997

INT-CL (IPC): H01L 23/12

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method for manufacturing a low-cost semiconductor package which is mounted on a small portable equipment, etc.

SOLUTION: In this method, a circuit board forming process, where an IC chip mounting wiring pattern and an electrode pattern for forming an external connection electrode are arrayed in a plurality on the surface of a collective circuit board 1A, an IC chip mounting process where the IC chip 6 is mounted on the wiring pattern, a resin sealing process where the IC chip 6 is sealed up with a sealing resin 7, a ball-fitting process where ball electrodes 9, and protruding electrodes, are formed at an external connection electrode, and a process where a protruding part is formed outside a package product, are provided to form a package aggregate. Furthermore, a holding process where the ball electrodes 9 of the package aggregate is fixed to a reference member, and a dicing process where the held package aggregate is cut along a cut line to form a single finished semiconductor package 10 are provided. This manufacturing method is optimum as a CSP(chip size/scale.package), and is superior in reliability and productivity.

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開平11－8330
(43)公開日　平成11年(1999)１月12日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　23/12		Ｈ０１Ｌ　23/12	Ｌ

審査請求　未請求　請求項の数９　ＯＬ　（全６頁）

(21)出願番号　特願平9－158689

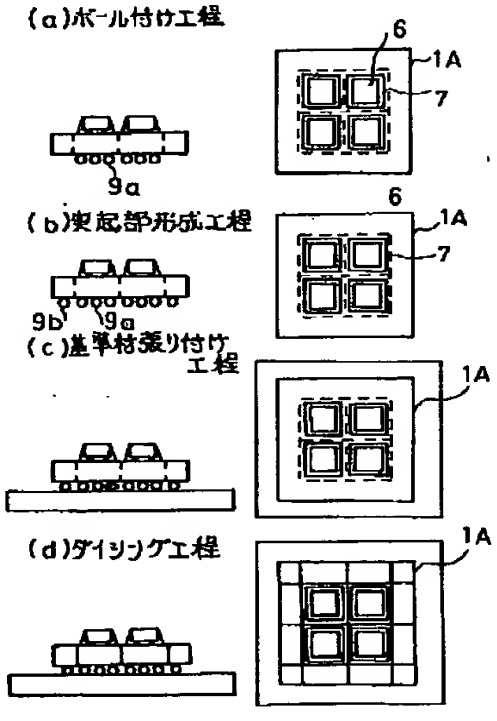
(22)出願日　平成９年(1997)６月16日

(71)出願人　000001960
シチズン時計株式会社
東京都新宿区西新宿２丁目１番１号
(72)発明者　石田　芳弘
東京都田無市本町６丁目１番12号　シチズン時計株式会社田無製造所内
(72)発明者　清水　潔
東京都田無市本町６丁目１番12号　シチズン時計株式会社田無製造所内
(72)発明者　佐藤　哲夫
東京都田無市本町６丁目１番12号　シチズン時計株式会社田無製造所内

最終頁に続く

(54)【発明の名称】　半導体パッケージの製造方法

(57)【要約】
【課題】　単個でボール付けは生産性が低い、生産コストが高くなる。
【解決手段】　ＩＣチップ実装用の配線パターンと外部接続用電極を形成するための電極パターンとを集合回路基板１Ａ面に複数個分配列して形成する回路基板形成工程と、前記配線パターンに前記ＩＣチップ６を実装するＩＣチップ実装工程と、ＩＣチップ５を封止樹脂７で封止する樹脂封止工程と、外部接続用電極に突起電極であるボール電極９ａを形成するボール付け工程とパッケージの製品外に突起部を形成する工程によりパッケージ集合体を形成し、パッケージ集合体のボール電極９を基準部８材に固定する保持工程と、保持されたパッケージ集合体をカットライン２に沿って切削して単個の完成半導体パッケージを形成するダイシング工程とよりなる半導体パッケージの製造方法である。ＣＳＰとして最適な製造方法で信頼性及び生産性が優れている。



1

【特許請求の範囲】

【請求項１】　ＩＣチップを実装した半導体パッケージの製造方法において、前記ＩＣチップ実装用のボンディングパターンと外部接続用電極を形成するための電極パターンとを集合回路基板面に複数個分配列して形成する回路基板形成工程と、前記ボンディングパターンと前記ＩＣチップを電気的接続するＩＣチップ実装工程と、該ＩＣチップを樹脂封止する封止工程と、前記外部接続用電極に突起電極を形成する電極形成工程と、前記回路基板の前記突起電極面のパッケージ製品外の面に突起部を形成する突起部形成工程によりパッケージ集合体を形成し、該パッケージ集合体の突起電極を基準部材に固定する保持工程と、保持されたパッケージ集合体の回路基板を切削して単個の完成半導体パッケージを形成する切削工程とからなることを特徴とする半導体パッケージの製造方法。

【請求項２】　前記突起部は、前記切削工程で切断された全ての個片に有ることを特徴とする請求項１記載の半導体パッケージの製造方法。

【請求項３】　前記突起部は、前記突起電極とほぼ同等の構造であることを特徴とする請求項１，２記載の半導体パッケージの製造方法。

【請求項４】　前記突起部形成工程と前記突起電極形成工程は、同じ工程で行われることを特徴とする請求項１～３記載の半導体パッケージの製造方法。

【請求項５】　前記突起部は、液状樹脂で構成されていることを特徴とする請求項１，２記載の半導体パッケージの製造方法。

【請求項６】　前記液状樹脂で構成された突起部は、線状に形成してあること特徴とする請求項５記載の半導体パッケージの製造方法。

【請求項７】　前記突起部は、平板を接着する構造であることを特徴とする請求項１，５記載の半導体パッケージの製造方法。

【請求項８】　前記突起部と前記突起電極の高さは、ほぼ同じであること特徴とする請求項１～７記載の半導体パッケージの製造方法。

【請求項９】　前記突起電極は、半田バンプであることを特徴とする請求項１～８記載の半導体パッケージの製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体パッケージの製造方法に係わり、更に詳しくは外部接続用の突起電極を有する半導体パッケージの製造方法に関するものである。

【０００２】

【従来の技術】近年、半導体パッケージの小型化、高密度化に伴いベア・チップを直接フェイスダウンで、基板上に実装するフリップチップボンディングが開発されて

2

いる。カメラ一体型ＶＴＲや携帯電話機等の登場により、ベア・チップと略同じ寸法の小型パッケージ、所謂ＣＳＰ（チップサイズ／スケール・パッケージ）を載せた携帯機器が相次いで登場してきている。最近ＣＳＰの開発は急速に進み、その市場要求が本格化している。

【０００３】図５は、多数個取りし、高密度実装化した従来技術が特開平８－１５３８１９号公報に開示されている。以下図面に基づいてその概要を説明する。

【０００４】図５において、短冊状の回路基板１にスルーホール２を形成後、銅メッキ層を施す工程と、全ての回路パターンと接続する共通電極１４を含む複数個、例えば２個のＢＧＡを構成する回路パターンを形成する回路パターン形成工程と、前記回路基板１の上下両面に感光性樹脂皮膜を施した後、エッチングにより、共通電極１４及びＩＣチップ、ボンディングワイヤ、半田バンプの各接続部を除くようにドライフイルムを形成するドライフイルムラミネート工程と、前記共通電極１４を利用して前記回路基板１の上下両面の露出している電極の銅メッキ層の表面に、Ｎｉ－Ａｕメッキ層を形成する。

【０００５】次に、共通電極１４と回路パターンとを分離するパターン分離工程は、製品分離ライン１５の四辺に沿って、その四隅に回路基板１と連結する連結部１５ａを残すように、ルータ加工により長穴１６を穴明けする。その後、ワイヤーボンディング及びトランスファーモールドにより樹脂封止し、回路基板１の下面に半田バンプを形成する。

【０００６】製品分離工程は、前記四隅に残した連結部は狭隘なため、プレス抜き等の切り離し手段で余分な負荷をかけることなく極めて容易に分離することにより、単個のＢＧＡを製造することができる。

【０００７】しかしながら、前述した短冊状の複数個取りする半導体パッケージの製造方法は、単個の半導体パッケージの製造方法に比較して生産性は若干向上するが、小型パッケージであるＣＳＰにおいては、回路基板製造時の基板取り個数が少なく、生産コストが高くなる。また、前記ＣＳＰのように、前記回路基板の外縁から最外周に位置するボール電極の中心までの距離が差が無くなると、製品分離工程でプレス抜き等の切り離し手段で分離する時の金型押さえ代が無くなる等の問題があった。

【０００８】そこで、小型携帯機器等に搭載するＣＳＰの従来の半導体パッケージの製造方法について以下その概要を説明する。

【０００９】先ず図６（ａ）に示す多数個取りする回路基板形成工程は、両面銅張りされた集合回路基板１Ａにスルーホール（図示しない）を形成した後、無電解銅メッキ及び電解銅メッキにより銅メッキ層を形成し、更にメッキレジストをラミネートし、露光現像してパターンマスクを形成した後、エッチング液を用いてパターンエッチングを行うことにより、前記集合回路基板１Ａの上

面側には複数個分配列したＩＣ接続用電極３、下面側にパッド電極である外部接続用電極４を形成する。次にソルダーレジスト処理を行い、所定の部分にレジスト膜を形成することにより、前記集合回路基板１Ａの下面側には外部接続用電極４を露呈するように、マトリックス状に多数の同一形状の半田付け可能な表面であるレジスト膜の開口部を形成し、多数個取りする集合回路基板１Ａが完成される。２はＸ、Ｙ方向に直交するカットラインである。

【００１０】図６（ｂ）に示すＩＣチップ実装工程は、先ず、ＩＣウエハーをバンプ工程に流して前記ＩＣウエハーのパッド電極面に半田バンプ５を形成する。前記半田バンプ５の形成方法には、一般に、スタッドバンプ方式、ボールバンプ方式、及びメッキバンプ方式等があるが、その中で、パッド電極位置にレジストにて窓を形成し半田浴槽中に浸漬してメッキにて半田バンプを形成するメッキバンプ方式は、パッド電極間の狭い配列でバンプを形成することが可能で、ＩＣチップの小型化には有効な半田バンプの形成手段である。

【００１１】前記半田バンプ５を形成後、前記ＩＣウエハーを粘着テープ等で貼着した状態で、所定のチップサイズにダイシングソー等の装置でウエハーの厚みをフルカット方式でＸ、Ｙ方向に切断した後、ＩＣチップ６を単体に分割する。

【００１２】前記半田バンプ付きＩＣチップ６、又は前述した集合回路基板１Ａの前記配線パターンの所定位置にフラックスを塗布して、単体に分割した前記ＩＣチップ６を１個づつ複数個分配列した集合回路基板１Ａの個々の回路基板１上の所定位置に搭載した後、半田リフロー工程を経て、フリップチップ実装を行う。

【００１３】図６（ｃ）に示す封止工程は、熱硬化性の封止樹脂７で前記隣接する複数個のＩＣチップ５に跨がった状態で、サイドポッティングにより一体的に樹脂封止することにより、ＩＣチップ６はフェイスダウンで集合回路基板１Ａの個々の回路基板１上に固定される。

【００１４】図７（ａ）に示すボール付け工程は、ＩＣチップ６を実装した集合回路基板１Ａの下面側に形成された外部接続用電極４の位置に、半田ボールを配置してリフローすることによりボール電極９を形成する。

【００１５】図７（ｂ）に示す基準部材張り付け工程は、ＩＣチップ６を実装した集合回路基板１Ａの下面側に形成された外部接続用電極４を、基準部材８上に接着剤又は粘着テープ等の固定手段で張り付ける。

【００１６】図７（ｃ）は、タイシング工程で、前述のＸ、Ｙ方向のカットライン２に沿って、ダイシングソー等の切削手段で単個に切削、分割した後、熱等により基準部材８より剥離する。

【００１７】

【発明が解決しようとする課題】しかしながら、前述した半導体パッケージの製造方法には次のような問題点がある。即ち、ダイシング工程で単個に切削、分割されたとき、製品外の回路基板も同様に分割される。

このとき、製品外の回路基板は基準部材８上に固定されていないため、切削時、分離された基板片がダイシング機内で飛びはね、ダイシングブレードが破損する等の問題があった。

【００１８】本発明は、上記従来の課題に鑑みなされたものであり、その目的は、小型携帯機器等に搭載する安価な半導体パッケージの製造方法を提供するものである。

【００１９】

【課題を解決するための手段】上記目的を達成するために、本発明における半導体パッケージの製造方法は、ＩＣチップを実装した半導体パッケージの製造方法において、前記ＩＣチップ実装用のボンディングパターンと外部接続用電極を形成するための電極パターンとを集合回路基板面に複数個分配列して形成する回路基板形成工程と、前記ボンディングパターンと前記ＩＣチップを電気的接続するＩＣチップ実装工程と、該ＩＣチップを樹脂封止する封止工程と、前記外部接続用電極に突起電極を形成する電極形成工程と、前記回路基板の前記突起電極面のパッケージ製品外の面に突起部を形成する突起部形成工程によりパッケージ集合体を形成し、該パッケージ集合体の突起電極を基準部材に固定する保持工程と、保持されたパッケージ集合体の回路基板を切削して単個の完成半導体パッケージを形成する切削工程とからなることを特徴とするものである。

【００２０】また、前記突起部は、突起部は前記切削工程で切断された全ての個片に有ることを特徴とするものである。

【００２１】また、前記突起部は、前記突起電極とほぼ同等の構造であることを特徴とするものである。

【００２２】また、前記突起部形成工程と前記突起電極形成工程は、同じ工程で行われることを特徴とするものである。

【００２３】また、前記突起部は、液状樹脂で構成されていることを特徴とするものである。

【００２４】また、前記液状樹脂で構成された突起部は、線状に形成してあること特徴とするものである。

【００２５】また、前記突起部は、平板を接着する構造であることを特徴とするものである。

【００２６】また、前記突起部と前記突起電極の高さは、ほぼ同じであること特徴とするものである。

【００２７】また、前記突起電極は、半田バンプであることを特徴とするものである。

【００２８】

【発明の実施の形態】以下図面に基づいて本発明における半導体パッケージの製造方法について説明する。図１及び図２は本発明の実施の形態で、突起電極付きの半導体パッケージの製造工程を示す説明図である。従来技術

と同一部材は同一符号で示す。

【００２９】先ず、図１（ａ）の回路基板形成工程、図１（ｂ）のＩＣ実装工程、図１（ｃ）の樹脂封止工程は、前述の従来技術と同様であるので、説明は省略する。

【００３０】図２（ａ）に示すボール電極を形成するボール付け工程は、前記集合回路基板１Ａの個々の回路基板１の下面側に形成された外部接続用電極４ａの位置に、半田ボールを配置してリフローすることにより突起電極であるボール電極９ａが形成される。

【００３１】図２（ｂ）に示す突起部形成工程は、前記集合回路基板１Ａの個々の回路基板１の下面側に形成されたボール電極９ａ面にあるパッケージ製品外の突起形成パッド４ｂの位置に、半田ボールを配置してリフローすることにより半田ボール突起部９ｂが形成される。

【００３２】図２（ｃ）に示す基準部材張り付け工程は、ボール電極９ａ及び半田ボール突起部９ｂを基準部材８に接着剤、例えば、日東電工（株）製の熱剥離テープ「エレップホルダー感圧型ダイシングテープ、ＳＰＶ－２２４」等の固定手段により張りつけることで、基準部材８上に固定する。

【００３３】図２（ｄ）はタイシング工程で、前述のＸ、Ｙ方向のカットライン２に沿って、ダイシングソー、例えば、ディスコ製のダイシング機「ＤＦＤ－６４０」、使用ブレード「ＮＢＣ－ＺＢ１０９０Ｓ３、０．１ｍｍ幅」等を使用した切削手段で単個に切削、分割した後、熱により前述剥離テープの接着力を低下させた後、基準部材８より剥離する。以上の工程により単個のフリップチップＢＧＡ１０が完成される。

【００３４】図３（ａ）は、パッケージ製品外の突起部形成工程を液状樹脂により構成した時のボール電極面より見た図である。

図３（ｂ）は、図３（ａ）のＡ－Ａ‘断面図である。

【００３５】液状樹脂突起９ｃは液状樹脂をディスペンサー等により集合回路基板１ａの製品外に塗布した後、熱またはＵＶ等により硬化させることで形成できる。

【００３６】図４（ａ）は、パッケージ製品外の突起部形成工程を平板により構成した時のボール電極面面より見た図である。

【００３７】図４（ｂ）は、図４（ａ）のＢ－Ｂ’断面図である。

【００３８】平板突起９ｄは平板を両面接着剤等により集合回路基板１ａの製品外に接着して形成できる。

【発明の効果】以上説明したように、本発明の半導体パッケージの製造方法によれば、前記集合回路基板の上面側に複数個分配列して回路基板にＩＣチップを実装し、封止樹脂でサイドモールドして、下面側の外部接続用電極に突起電極を形成し、パッケージ製品外の面に突起部を形成した後、突起電極と突起部を基準部材に固定した後、切削して単個の半導体パッケージを製造することにより、小型携帯機器等に搭載する信頼性及び生産性の優れた半導体パッケージの製造方法を提供することが可能である。

【図面の簡単な説明】

【図１】本発明の実施の形態に係わる半導体パッケージの製造工程で、回路基板形成工程、ＩＣ実装工程、樹脂封止工程を示す説明図である。

【図２】図１の製造工程後のボール付け工程、突起部形成工程、基準部材張り付け工程、ダイシング工程を示す説明図である。

【図３】突起部を液状樹脂により構成した図の平面図と断面図である。

【図４】突起部を平板により構成した図の平面図と断面図である。る。

【図５】従来の短冊状のＢＧＡの平面図である。

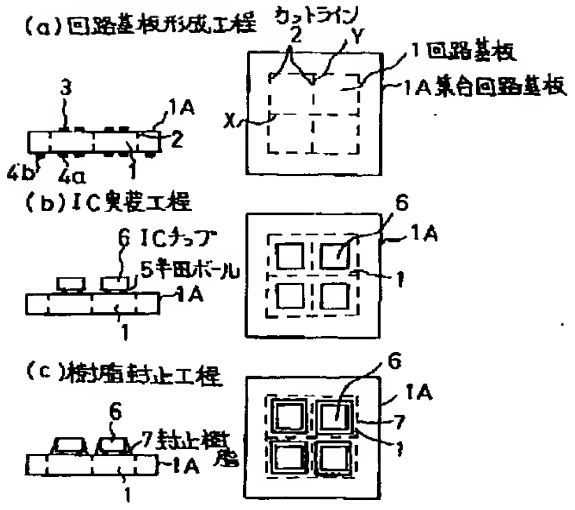
【図６】従来のＢＧＡの製造工程で、回路基板形成工程、ＩＣ実装工程、樹脂封止工程を示す説明図である。

【図７】従来のＢＧＡの製造工程で、図５の製造工程後のボール付け工程、基準部材張り付け工程、ダイシング工程を示す説明図である。

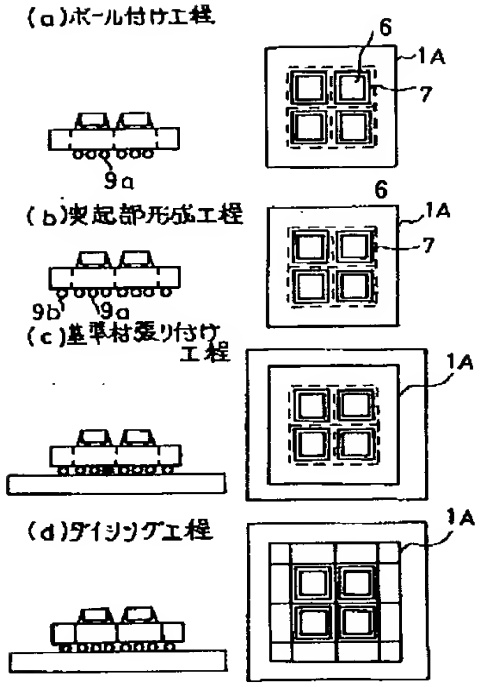
【符号の説明】

１　回路基板
１Ａ　集合回路基板
２　カットライン
３　ＩＣ接続用電極
４ａ　外部接続用電極
４ｂ　突起形成パッド
５　半田ボール
６　ＩＣチップ
７　封止樹脂
８　基準部材
９ａ　ボール電極（突起電極）
９ｂ　突起部（ボール）
９ｃ　突起部（液状樹脂）
９ｄ　突起部（平板）
１０　フリップチップＢＧＡ

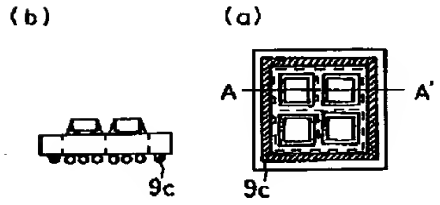
【図1】



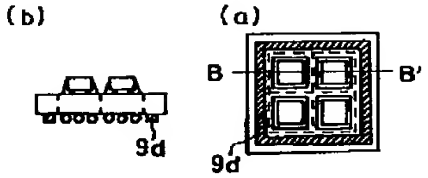
【図2】



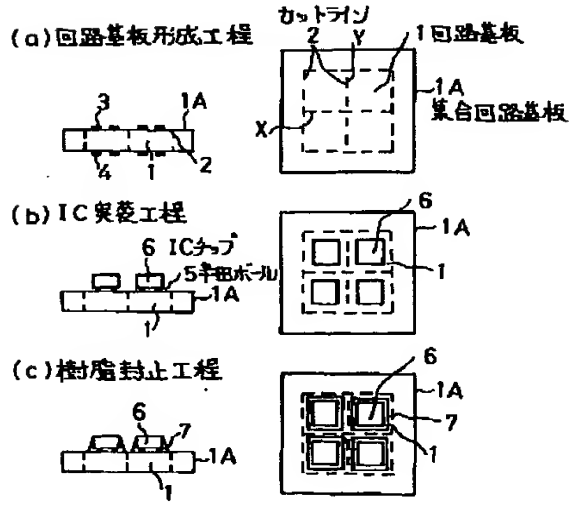
【図3】



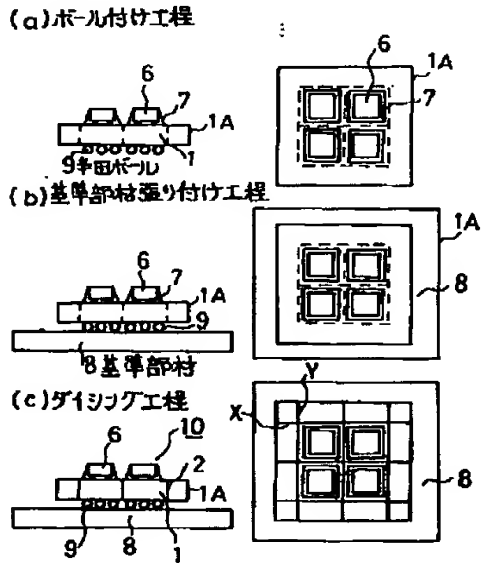
【図4】



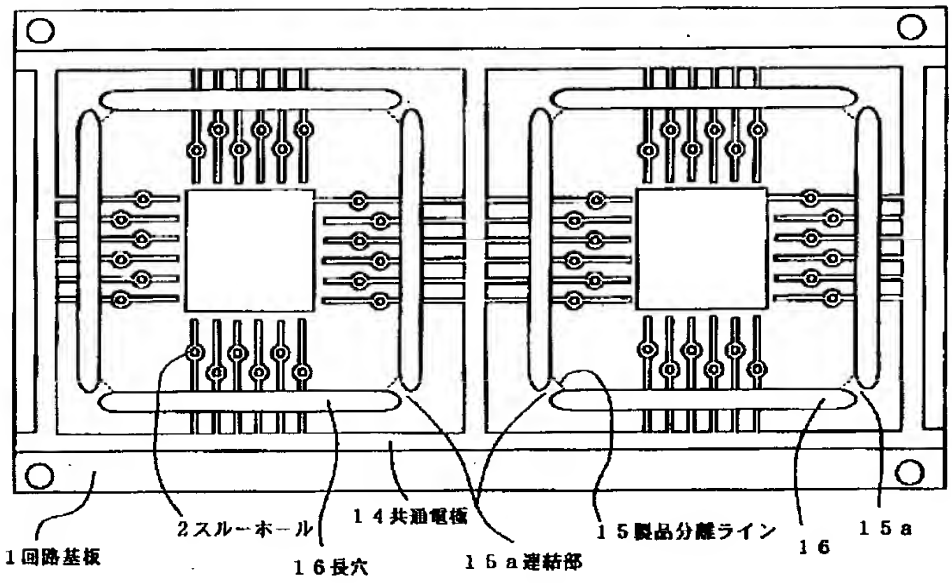
【図6】



【図7】



【図５】



フロントページの続き

(72)発明者　西方　進一
東京都田無市本町６丁目１番12号　シチズン時計株式会社田無製造所内

(72)発明者　大原　務
埼玉県所沢市大字下富字武野840番地　シチズン時計株式会社技術研究所内

Pat Family in STN

>
MANUFACTURE FOR SEMICONDUCTOR PACKAGE (English)
Patent Assignee: CITIZEN WATCH CO LTD
Author (Inventor): ISHIDA YOSHIHIRO; SHIMIZU KIYOSHI; SATO TETSUO; NISHIKATA SHINICHI; KOMURA ATSUSHI
IPC: *H01L-023/12; H01L-021/301
CA Abstract No: *130(04)046167R; 130(04)046167R
Derwent WPI Acc No: *G 99-010065;
Language of Document: Japanese
Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date	
CN 1225750	T	19990811	CN 98800579	A	19980424	
EP 932198	A1	19990728	EP 98917679	A	19980424	
JP 10308473	A2	19981117	JP 97119220	A	19970509	(BASIC)
JP 11008329	A2	19990112	JP 97158688	A	19970616	
JP 11008330	A2	19990112	JP 97158689	A	19970616	
JP 11097579	A2	19990409	JP 97256503	A	19970922	
JP 11135557	A2	19990521	JP 97295317	A	19971028	
WO 9852220	A1	19981119	WO 98JP1905	A	19980424	
TW 395033	B	20000621	TW 87106959	A	19980506	

Priority Data (No,Kind,Date):

JP 97119220	A	19970509
JP 97158688	A	19970616
JP 97158689	A	19970616
JP 97256503	A	19970922
JP 97295317	A	19971028
WO 98JP1905	W	19980424

?

CLAIMS

[Claim(s)]
[Claim 1] The circuit board formation process which carries out the distribution train of two or more electrode patterns for forming the bonding pattern for the aforementioned IC chip package, and the electrode for external connection to a set circuit board side, and forms them in it in the manufacture technique of the semiconductor package which mounted IC chip, IC chip package process which carries out electrical installation of the aforementioned IC chip to the aforementioned bonding pattern, The closure process which carries out the resin seal of this IC chip, and the electrode formation process which forms a salient electrode in the aforementioned electrode for external connection, The hold process which forms the package aggregate according to the height formation process which forms a height in the field besides the package product of the aforementioned salient electrode side of the aforementioned circuit board, and fixes the salient electrode of this package aggregate to a criteria member, The manufacture technique of the semiconductor package characterized by consisting of a cutting process which cuts the circuit board of the held package aggregate and forms the completion semiconductor package of a single individual.
[Claim 2] The aforementioned height is the manufacture technique of the semiconductor package according to claim 1 characterized by being in all the pieces of an individual cut at the aforementioned cutting process.
[Claim 3] The aforementioned height is the manufacture technique of the semiconductor package a claim 1 and two publications characterized by being structure almost equivalent to the aforementioned salient electrode.
[Claim 4] The aforementioned height formation process and the aforementioned salient electrode formation process are the manufacture technique of the semiconductor package according to claim 1 to 3 characterized by being carried out at the same process.
[Claim 5] The aforementioned height is the manufacture technique of the semiconductor package a claim 1 and two publications characterized by consisting of a liquefied resin.
[Claim 6] The height which consisted of an aforementioned liquefied resin is the manufacture technique of the semiconductor package according to claim 5 by which it is forming [in a line] characterized.
[Claim 7] The aforementioned height is the manufacture technique of the semiconductor package a claim 1 and five publications characterized by being the structure of pasting up a plate.
[Claim 8] The height of the aforementioned height and the aforementioned salient electrode is the manufacture technique of the semiconductor package according to claim 1 to 7 by which it is things characterized [almost same].
[Claim 9] The aforementioned salient electrode is the manufacture technique of the semiconductor package according to claim 1 to 8 characterized by being a solder bump.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture technique of the semiconductor package which has a still detailed salient electrode for external connection with respect to the manufacture technique of a semiconductor package.
[0002]
[Description of the Prior Art] In recent years, the flip chip bonding which mounts a bare chip on a substrate by direct face down in connection with a miniaturization of a semiconductor package and high-density-izing is developed. an appearance of a camcorder/movie, a portable telephone, etc. -- a bare chip and abbreviation -- the same compact package of a dimension and the pocket device which carried the so-called CSP (a chip size / scale package) have appeared successively Recently, a development of CSP progresses quickly and the commercial-scene demand has got into stride.
[0003] The conventional technique which took much drawings 5 , carried out and was high-density-assembly-ized is indicated by JP,8-153819,A. Based on a drawing, the schema is explained below.
[0004] The process which gives a copper-coating layer to the strip-of-paper-like circuit board 1 after forming a through hole 2 in drawing 5 , After giving a photopolymer coat to the circuit pattern formation process which forms the circuit pattern containing the common electrode 14 linked to all circuit patterns which constitutes two BGA two or more, and vertical both sides of the aforementioned circuit board 1, by etching The common electrode 14 and IC chip, a bonding wire, and the dry film lamination process that forms a dry film so that each connection of a solder bump may be removed, A nickel-Au deposit is formed in the front face of the copper-coating layer of the electrode which has exposed vertical both sides of the aforementioned circuit board 1 using the aforementioned common electrode 14.
[0005] Next, the pattern separation process of separating the common electrode 14 and a circuit pattern carries out hole dawn of the slot 16 by router manipulation so that it may leave link section 15a connected with the circuit board 1 in the four corners along with the neighborhood of the product separation line 15. Then, a resin seal is carried out by wire bonding and the transfer mold, and a solder bump is formed in the inferior surface of tongue of the circuit board 1.
[0006] Since the link section which left the product separation process to the aforementioned four corners is narrow, it can manufacture BGA of a single individual by dissociating very easily, without applying an excessive load with separation meanses, such as punching.
[0007] However, although the productivity of manufacture technique of the semiconductor package of the shape of a strip of paper mentioned above which takes and is carried out improves a little as compared with the manufacture technique of the semiconductor package of a single individual, in CSP which is a compact package, there is little base blanking number at the time of a circuit board manufacture, and a production cost becomes high. [two or more] Moreover, when the distance of a difference to the center of a ball electrode of being located in the outermost periphery from the rim of the aforementioned circuit board was lost like aforementioned CSP, there was a problem of a grade that ** even of a golden die pressing in case separation meanses, such as punching, separate at a product separation process was lost.
[0008] Then, the schema is explained below about the manufacture technique of the conventional semiconductor package of CSP carried in a small pocket device etc.
[0009] The circuit board formation process which is first shown in drawing 6 (a) and which takes and is carried out [many] After forming a through hole (not shown) in set circuit board 1A by which the double-sided copper flare was carried out, After forming a copper-coating layer by non-electrolytic-copper plating and electrolytic-copper plating, laminating and carrying out exposure development of the plating resist further and forming a pattern mask, by performing pattern etching using an etching reagent The electrode for external connection 4 which is a pad electrode is formed in an electrode [which carried out the distribution train to the top side of the aforementioned set circuit board 1A] 3 for IC connection, and inferior-surface-of-tongue side. Next, solder resist processing is performed, by forming a resist layer in a predetermined fraction, opening of the resist layer which is the front face which can solder many same configurations is formed in the shape of a matrix, and set circuit board 1A which takes and is carried out is completed at the inferior-surface-of-tongue side of the aforementioned set circuit board 1A so that the electrode for external connection 4 may be exposed. [much] 2 is a cutline which intersects perpendicularly in X and the orientation of Y.
[0010] First, IC chip package process shown in drawing 6 (b) pours IC wafer at a bump process, and forms the solder bump 5 in the pad electrode side of the aforementioned IC wafer. Although a stud bump method, a ball bump method, a plating bump method, etc. are generally in the aforementioned solder bump's 5 formation technique, the plating bump method which forms an aperture in a pad electrode position in a resist, is immersed into a solder bathtub in it, and forms a solder bump by plating can form a bump in a pad inter-electrode narrow array, and is the formation means of a solder bump effective in a miniaturization of IC chip.
[0011] Where the aforementioned IC wafer is stuck by the adhesive tape etc. after forming the aforementioned solder bump 5, after the equipment of a dicing saw etc. cut to the predetermined chip size and a full cutting method cuts the thickness of a wafer in X and the orientation of Y, the IC chip 6 is divided into a simple substance.
[0012] Flux is applied to the aforementioned IC chip with a solder bump 6, or the predetermined position of aforementioned

wiring Bataan of set circuit board 1A mentioned above, after carrying in the predetermined position on the circuit board 1 of each of set circuit board 1A which carried out the distribution train of two or more every one aforementioned IC chip 6 divided into the simple substance, it passes through a solder reflow process and a flip chip package is performed.
[0013] The closure process shown in drawing 6 (c) is in the status over two or more aforementioned IC chips 5 which carry out contiguity by the thermosetting closure resin 7, and the IC chip 6 is fixed on the circuit board 1 of each of set circuit board 1A by face down by carrying out a resin seal in one by side potting.
[0014] The ball attachment process shown in drawing 7 (a) forms the ball electrode 9 in the position of the electrode for external connection 4 formed in the inferior-surface-of-tongue side of set circuit board 1A which mounted the IC chip 6 by arranging and carrying out a reflow of the solder ball.
[0015] The criteria member attachment process shown in drawing 7 (b) sticks the electrode for external connection 4 formed in the inferior-surface-of-tongue side of set circuit board 1A which mounted the IC chip 6 with fixed meanses, such as adhesives or an adhesive tape, on the criteria member 8.
[0016] Drawing 7 (c) is a tie ****** process, and after meeting the above-mentioned X and the cutline 2 of the orientation of Y and cutting and dividing into a single individual with cutting meanses, such as a dicing saw, it exfoliates from the criteria member 8 with heat etc.
[0017]
[Problem(s) to be Solved by the Invention] However, there are the following troubles in the manufacture technique of a semiconductor package mentioned above. That is, when it is cut by the single individual and it is divided into it at a dicing process, the circuit board besides a product is divided similarly. Since the circuit board besides a product was not being fixed on the criteria member 8 at this time, there was a problem of a dicing blade being damaged in a jump by the dicing inside of a plane by the separated piece of a substrate at the time of cutting. [0018] this invention is made in view of the above-mentioned conventional technical probrem, and the purpose offers the manufacture technique of the cheap semiconductor package carried in a small pocket device etc.
[0019]
[Means for Solving the Problem] The manufacture technique of a semiconductor [this invention] package for attaining the above-mentioned purpose The circuit board formation process which carries out the distribution train of two or more electrode patterns for forming the bonding pattern for the aforementioned IC chip package, and the electrode for external connection to a set circuit board side, and forms them in it in the manufacture technique of the semiconductor package which mounted IC chip, IC chip package process which carries out electrical installation of the aforementioned IC chip to the aforementioned bonding pattern, The closure process which carries out the resin seal of this IC chip, and the electrode formation process which forms a salient electrode in the aforementioned electrode for external connection, The hold process which forms the package aggregate according to the height formation process which forms a height in the field besides the package product of the aforementioned salient electrode side of the aforementioned circuit board, and fixes the salient electrode of this package aggregate to a criteria member, It is characterized by consisting of a cutting process which cuts the circuit board of the held package aggregate and forms the completion semiconductor package of a single individual.
[0020] Moreover, it is characterized by the aforementioned height having a height in all the pieces of an individual cut at the aforementioned cutting process.
[0021] Moreover, it is characterized by the aforementioned height being structure almost equivalent to the aforementioned salient electrode.
[0022] Moreover, it is characterized by performing the aforementioned height formation process and the aforementioned salient electrode formation process at the same process.
[0023] Moreover, it is characterized by the aforementioned height consisting of a liquefied resin.
[0024] Moreover, it is forming [in a line] characterized by the height which consisted of an aforementioned liquefied resin.
[0025] Moreover, it is characterized by the aforementioned height being the structure of pasting up a plate.
[0026] Moreover, it is things characterized [almost same] by the height of the aforementioned height and the aforementioned salient electrode.
[0027] Moreover, it is characterized by the aforementioned salient electrode being a solder bump.
[0028]
[Embodiments of the Invention] Based on a drawing, the manufacture technique of a semiconductor package in this invention is explained below. The drawing 1 and the drawing 2 are the gestalt of operation of this invention, and are explanatory drawing showing the manufacturing process of the semiconductor package with a salient electrode. The same sign shows the same member as the conventional technique.
[0029] First, since the circuit board formation process of drawing 1 (a), IC package process of drawing 1 (b), and the resin-seal process of drawing 1 (c) are the same as that of the above-mentioned conventional technique, an explanation is omitted.
[0030] When the ball attachment process which forms the ball electrode shown in drawing 2 (a) arranges and carries out a reflow of the solder ball to the position of electrode 4a for external connection formed in the inferior-surface-of-tongue side of each circuit board 1 of the aforementioned set circuit board 1A, ball electrode 9a which is a salient electrode is formed.
[0031] When the height formation process shown in drawing 2 (b) arranges and carries out a reflow of the solder ball to the position of salient formation pad 4b besides the package product in the ball electrode 9a page formed in the inferior-surface-of-tongue side of each circuit board 1 of the aforementioned set circuit board 1A, solder ball height 9b is formed.
[0032] The criteria member attachment process shown in drawing 2 (c) is sticking ball electrode 9a and solder ball height 9b on the criteria member 8 by fixed meanses, such as the adhesives by NITTO DENKO CORP., for example, a heat sublation tape etc., "a ******** electrode-holder pressure sensitivity type dicing tape and SPV-224", and is fixed on the criteria member 8.
[0033] Drawing 2 (d) is a tie ****** process, and after cutting and dividing into a single individual along with the above-mentioned X and the cutline 2 of the orientation of Y with the cutting means which used the dicing-saw, for example, disco dicing, machine "DFD-640" use blade "NBC-ZB1090S3 or 0.1mm width of face" etc. and reducing the adhesive power

of the above-mentioned sublation tape with heat, it exfoliates from the criteria member 8. Flip chip BGA10 of a single individual is completed by the above process.
[0034] Drawing 3 (a) is drawing seen from the ball electrode side when a liquefied resin constitutes the height formation process besides a package product. Drawing 3 (b) is an A-A' cross section of drawing 3 (a).
[0035] After liquefied resin salient 9c applies a liquefied resin out of the product of set circuit board 1a by the wire dispenser etc., it can be formed by making it harden by heat or UV. [0036] Drawing 4 (a) is drawing seen from ball electrode each one when constituting the height formation process besides a package product more monotonously. [0037] Drawing 4 (b) is a B-B' cross section of drawing 4 (a).
[0038] 9d of monotonous salients pastes up out of the product of set circuit board 1a with double-sided adhesives etc., and they can form a plate. [Effect of the Invention] As explained above, according to the manufacture technique of the semiconductor package of this invention Carry out the distribution train of the more than one to the top side of the aforementioned set circuit board, and mount IC chip in the circuit board and a side mould is carried out by the closure resin. By cutting and manufacturing the semiconductor package of a single individual, after forming a salient electrode in the electrode for external connection by the side of a inferior surface of tongue, forming a height in the field besides a package product and fixing a salient electrode and a height to a criteria member It is possible to offer the manufacture technique of the semiconductor package which was excellent in the reliability carried in a small pocket device etc. and the productivity.

[Translation done.]

Technique

[Description of the Prior Art] In recent years, the flip chip bonding which mounts a bare chip on a substrate by direct face down in connection with a miniaturization of a semiconductor package and high-density-izing is developed. an appearance of a camcorder/movie, a portable telephone, etc. -- a bare chip and abbreviation -- the same compact package of a dimension and the pocket device which carried the so-called CSP (a chip size / scale package) have appeared successively Recently, a development of CSP progresses quickly and the commercial-scene demand has got into stride.
[0003] The conventional technique which took much drawings 5 , carried out and was high-density-assembly-ized is indicated by JP,8-153819,A. Based on a drawing, the schema is explained below.
[0004] The process which gives a copper-coating layer to the strip-of-paper-like circuit board 1 after forming a through hole 2 in drawing 5 , After giving a photopolymer coat to the circuit pattern formation process which forms the circuit pattern containing the common electrode 14 linked to all circuit patterns which constitutes two BGA two or more, and vertical both sides of the aforementioned circuit board 1, by etching The common electrode 14 and IC chip, a bonding wire, and the dry film lamination process that forms a dry film so that each connection of a solder bump may be removed, A nickel-Au deposit is formed in the front face of the copper-coating layer of the electrode which has exposed vertical both sides of the aforementioned circuit board 1 using the aforementioned common electrode 14.
[0005] Next, the pattern separation process of separating the common electrode 14 and a circuit pattern carries out hole dawn of the slot 16 by router manipulation so that it may leave link section 15a connected with the circuit board 1 in the four corners along with the neighborhood of the product separation line 15. Then, a resin seal is carried out by wire bonding and the transfer mold, and a solder bump is formed in the inferior surface of tongue of the circuit board 1.
[0006] Since the link section which left the product separation process to the aforementioned four corners is narrow, it can manufacture BGA of a single individual by dissociating very easily, without applying an excessive load with separation meanses, such as punching.
[0007] However, although the productivity of manufacture technique of the semiconductor package of the shape of a strip of paper mentioned above which takes and is carried out improves a little as compared with the manufacture technique of the semiconductor package of a single individual, in CSP which is a compact package, there is little base blanking number at the time of a circuit board manufacture, and a production cost becomes high. [two or more] Moreover, when the distance of a difference to the center of a ball electrode of being located in the outermost periphery from the rim of the aforementioned circuit board was lost like aforementioned CSP, there was a problem of a grade that ** even of a golden die pressing in case separation meanses, such as punching, separate at a product separation process was lost.
[0008] Then, the schema is explained below about the manufacture technique of the conventional semiconductor package of CSP carried in a small pocket device etc.
[0009] The circuit board formation process which is first shown in drawing 6 (a) and which takes and is carried out [many] After forming a through hole (not shown) in set circuit board 1A by which the double-sided copper flare was carried out, After forming a copper-coating layer by non-electrolytic-copper plating and electrolytic-copper plating, laminating and carrying out exposure development of the plating resist further and forming a pattern mask, by performing pattern etching using an etching reagent The electrode for external connection 4 which is a pad electrode is formed in an electrode [which carried out the distribution train to the top side of the aforementioned set circuit board 1A] 3 for IC connection, and inferior-surface-of-tongue side. Next, solder resist processing is performed, by forming a resist layer in a predetermined fraction, opening of the resist layer which is the front face which can solder many same configurations is formed in the shape of a matrix, and set circuit board 1A which takes and is carried out is completed at the inferior-surface-of-tongue side of the aforementioned set circuit board 1A so that the electrode for external connection 4 may be exposed. [much] 2 is a cutline which intersects perpendicularly in X and the orientation of Y.
[0010] First, IC chip package process shown in drawing 6 (b) pours IC wafer at a bump process, and forms the solder bump 5 in the pad electrode side of the aforementioned IC wafer. Although a stud bump method, a ball bump method, a plating bump method, etc. are generally in the aforementioned solder bump's 5 formation technique, the plating bump method which forms an aperture in a pad electrode position in a resist, is immersed into a solder bathtub in it, and forms a solder bump by plating can form a bump in a pad inter-electrode narrow array, and is the formation means of a solder bump effective in a miniaturization of IC chip.
[0011] Where the aforementioned IC wafer is stuck by the adhesive tape etc. after forming the aforementioned solder bump 5, after the equipment of a dicing saw etc. cut to the predetermined chip size and a full cutting method cuts the thickness of a wafer in X and the orientation of Y, the IC chip 6 is divided into a simple substance.
[0012] Flux is applied to the aforementioned IC chip with a solder bump 6, or the predetermined position of aforementioned wiring Bataan of set circuit board 1A mentioned above, after carrying in the predetermined position on the circuit board 1 of each of set circuit board 1A which carried out the distribution train of two or more every one aforementioned IC chip 6 divided into the simple substance, it passes through a solder reflow process and a flip chip package is performed.
[0013] The closure process shown in drawing 6 (c) is in the status over two or more aforementioned IC chips 5 which carry out contiguity by the thermosetting closure resin 7, and the IC chip 6 is fixed on the circuit board 1 of each of set circuit board 1A by face down by carrying out a resin seal in one by side potting.

[0014] The ball attachment process shown in drawing 7 (a) forms the ball electrode 9 in the position of the electrode for external connection 4 formed in the inferior-surface-of-tongue side of set circuit board 1A which mounted the IC chip 6 by arranging and carrying out a reflow of the solder ball.
[0015] The criteria member attachment process shown in drawing 7 (b) sticks the electrode for external connection 4 formed in the inferior-surface-of-tongue side of set circuit board 1A which mounted the IC chip 6 with fixed meanses, such as adhesives or an adhesive tape, on the criteria member 8.
[0016] Drawing 7 (c) is a tie ****** process, and after meeting the above-mentioned X and the cutline 2 of the orientation of Y and cutting and dividing into a single individual with cutting meanses, such as a dicing saw, it exfoliates from the criteria member 8 with heat etc.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

Effect

[Effect of the Invention] As explained above, according to the manufacture technique of the semiconductor package of this invention Carry out the distribution train of the more than one to the top side of the aforementioned set circuit board, and mount IC chip in the circuit board and a side mould is carried out by the closure resin. By cutting and manufacturing the semiconductor package of a single individual, after forming a salient electrode in the electrode for external connection by the side of a inferior surface of tongue, forming a height in the field besides a package product and fixing a salient electrode and a height to a criteria member It is possible to offer the manufacture technique of the semiconductor package which was excellent in the reliability carried in a small pocket device etc. and the productivity.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, there are the following troubles in the manufacture technique of a semiconductor package mentioned above. That is, when it is cut by the single individual and it is divided into it at a dicing process, the circuit board besides a product is divided similarly. Since the circuit board besides a product was not being fixed on the criteria member 8 at this time, there was a problem of a dicing blade being damaged in a jump by the dicing inside of a plane by the separated piece of a substrate at the time of cutting. [0018] this invention is made in view of the above-mentioned conventional technical probrem, and the purpose offers the manufacture technique of the cheap semiconductor package carried in a small pocket device etc.

[Translation done.]

MEANS

[Means for Solving the Problem] The manufacture technique of a semiconductor [this invention] package for attaining the above-mentioned purpose The circuit board formation process which carries out the distribution train of two or more electrode patterns for forming the bonding pattern for the aforementioned IC chip package, and the electrode for external connection to a set circuit board side, and forms them in it in the manufacture technique of the semiconductor package which mounted IC chip, IC chip package process which carries out electrical installation of the aforementioned IC chip to the aforementioned bonding pattern, The closure process which carries out the resin seal of this IC chip, and the electrode formation process which forms a salient electrode in the aforementioned electrode for external connection, The hold process which forms the package aggregate according to the height formation process which forms a height in the field besides the package product of the aforementioned salient electrode side of the aforementioned circuit board, and fixes the salient electrode of this package aggregate to a criteria member, It is characterized by consisting of a cutting process which cuts the circuit board of the held package aggregate and forms the completion semiconductor package of a single individual.
[0020] Moreover, it is characterized by the aforementioned height having a height in all the pieces of an individual cut at the aforementioned cutting process.
[0021] Moreover, it is characterized by the aforementioned height being structure almost equivalent to the aforementioned salient electrode.
[0022] Moreover, it is characterized by performing the aforementioned height formation process and the aforementioned salient electrode formation process at the same process.
[0023] Moreover, it is characterized by the aforementioned height consisting of a liquefied resin.
[0024] Moreover, it is forming [in a line] characterized by the height which consisted of an aforementioned liquefied resin.
[0025] Moreover, it is characterized by the aforementioned height being the structure of pasting up a plate.
[0026] Moreover, it is things characterized [almost same] by the height of the aforementioned height and the aforementioned salient electrode.
[0027] Moreover, it is characterized by the aforementioned salient electrode being a solder bump.
[0028]
[Embodiments of the Invention] Based on a drawing, the manufacture technique of a semiconductor package in this invention is explained below. The drawing 1 and the drawing 2 are the gestalt of operation of this invention, and are explanatory drawing showing the manufacturing process of the semiconductor package with a salient electrode. The same sign shows the same member as the conventional technique.
[0029] First, since the circuit board formation process of drawing 1 (a), IC package process of drawing 1 (b), and the resin-seal process of drawing 1 (c) are the same as that of the above-mentioned conventional technique, an explanation is omitted.
[0030] When the ball attachment process which forms the ball electrode shown in drawing 2 (a) arranges and carries out a reflow of the solder ball to the position of electrode 4a for external connection formed in the inferior-surface-of-tongue side of each circuit board 1 of the aforementioned set circuit board 1A, ball electrode 9a which is a salient electrode is formed.
[0031] When the height formation process shown in drawing 2 (b) arranges and carries out a reflow of the solder ball to the position of salient formation pad 4b besides the package product in the ball electrode 9a page formed in the inferior-surface-of-tongue side of each circuit board 1 of the aforementioned set circuit board 1A, solder ball height 9b is formed.
[0032] The criteria member attachment process shown in drawing 2 (c) is sticking ball electrode 9a and solder ball height 9b on the criteria member 8 by fixed meanses, such as the adhesives by NITTO DENKO CORP., for example, a heat sublation tape etc., "a ******** electrode-holder pressure sensitivity type dicing tape and SPV-224", and is fixed on the criteria member 8.
[0033] Drawing 2 (d) is a tie ****** process, and after cutting and dividing into a single individual along with the above-mentioned X and the cutline 2 of the orientation of Y with the cutting means which used the dicing-saw, for example, disco dicing, machine "DFD-640" use blade "NBC-ZB1090S3 or 0.1mm width of face" etc. and reducing the adhesive power of the above-mentioned sublation tape with heat, it exfoliates from the criteria member 8. Flip chip BGA10 of a single individual is completed by the above process.
[0034] Drawing 3 (a) is drawing seen from the ball electrode side when a liquefied resin constitutes the height formation process besides a package product. Drawing 3 (b) is an A-A' cross section of drawing 3 (a).
[0035] After liquefied resin salient 9c applies a liquefied resin out of the product of set circuit board 1a by the wire dispenser etc., it can be formed by making it harden by heat or UV. [0036] Drawing 4 (a) is drawing seen from ball electrode each one when constituting the height formation process besides a package product more monotonously. [0037] Drawing 4 (b) is a B-B' cross section of drawing 4 (a).
[0038] 9d of monotonous salients pastes up out of the product of set circuit board 1a with double-sided adhesives etc., and they can form a plate.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the manufacturing process of the semiconductor package concerning the gestalt of operation of this invention, and is explanatory drawing showing a circuit board formation process, IC package process, and a resin-seal process.
[Drawing 2] It is explanatory drawing showing the ball attachment process after the manufacturing process of drawing 1 , a height formation process, a criteria member attachment process, and a dicing process.
[Drawing 3] It is the plan and cross section of drawing which constituted the height with the liquefied resin.
[Drawing 4] It is the plan and cross section of drawing which constituted the height more monotonously. **.
[Drawing 5] It is the plan of BGA of the shape of a conventional strip of paper.
[Drawing 6] It is explanatory drawing showing a circuit board formation process, IC package process, and a resin-seal process by the manufacturing process of the conventional BGA.
[Drawing 7] It is explanatory drawing showing the ball attachment process after the manufacturing process of drawing 5 , a criteria member attachment process, and a dicing process by the manufacturing process of the conventional BGA.
[Description of Notations]
1 Circuit Board
1A Set circuit board
2 Cutline
3 Electrode for IC Connection
4a The electrode for external connection
4b Salient formation pad
5 Solder Ball
6 IC Chip
7 Closure Resin
8 Criteria Member
9a Ball electrode (salient electrode)
9b Height (ball)
9c Height (liquefied resin)
9d Height (monotonous)
10 Flip Chip BGA

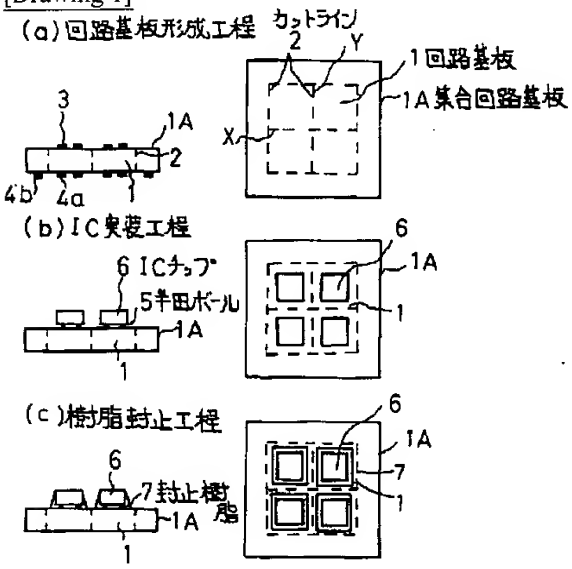
[Translation done.]

* NOTICES *

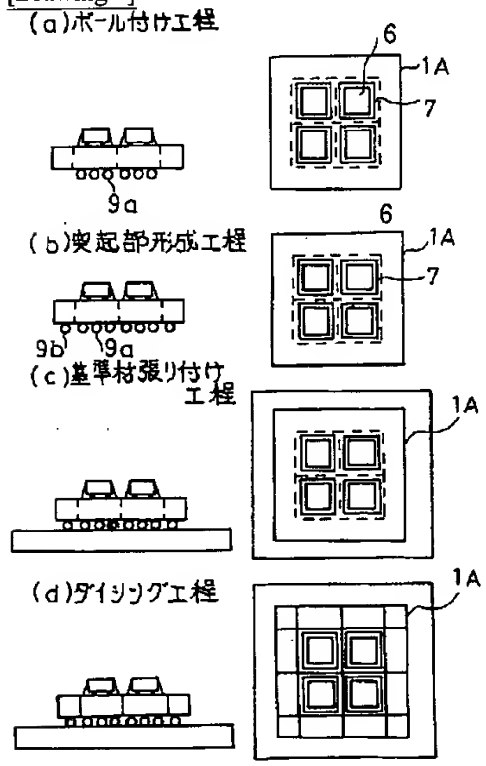
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

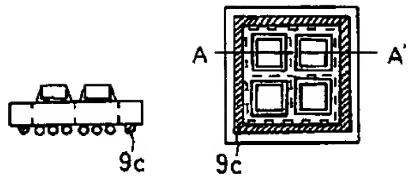


[Drawing 2]



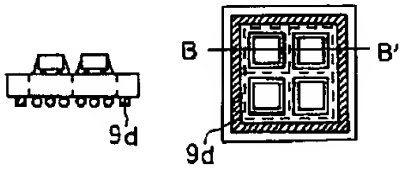
[Drawing 3]

(b) (a)



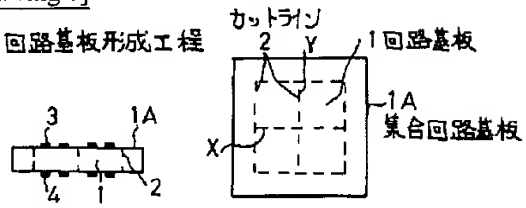
[Drawing 4]

(b) (a)

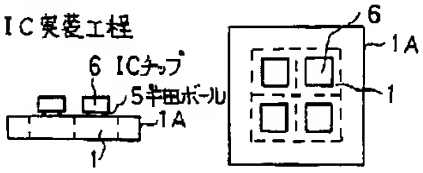


[Drawing 6]

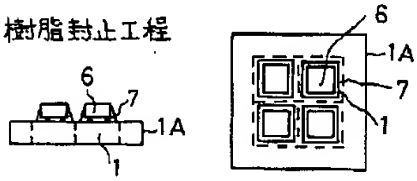
(a)回路基板形成工程



(b)IC実装工程

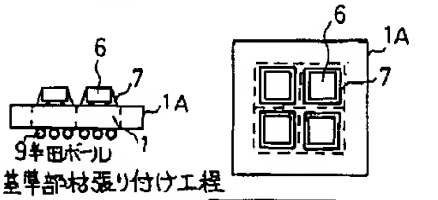


(c)樹脂封止工程

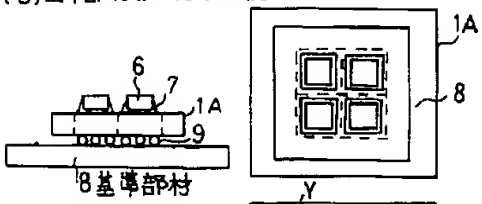


[Drawing 7]

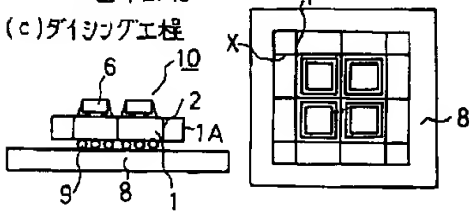
(a)ボール付け工程



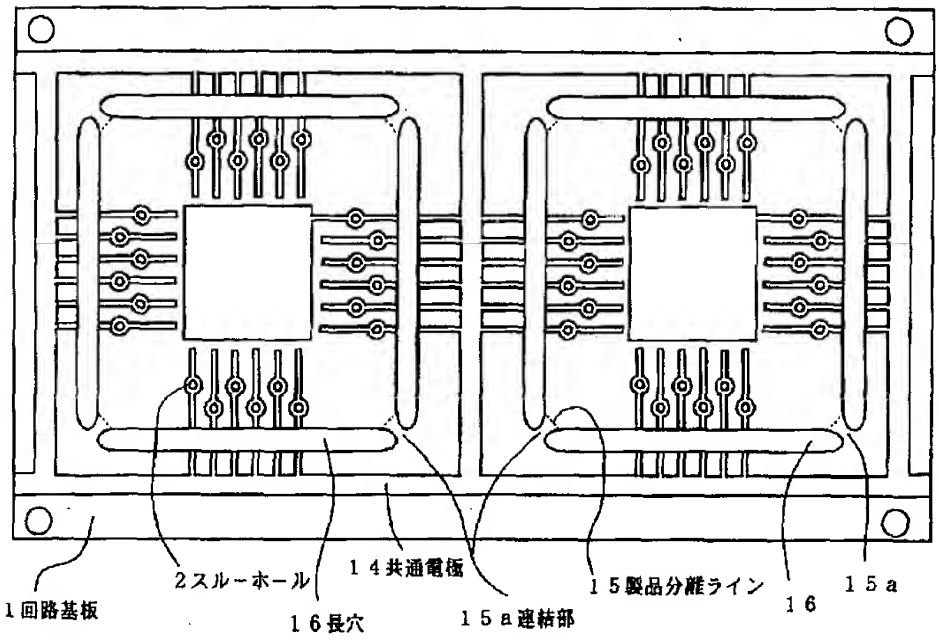
(b)基準部材張り付け工程



(c)ダイシング工程



[Drawing 5]



[Translation done.]

WEST

End of Result Set

☐ Generate Collection

L1: Entry 1 of 1 File: JPAB Apr 30, 1996

PUB-NO: JP408111470A
DOCUMENT-IDENTIFIER: JP 08111470 A
TITLE: BGA PACKAGE, MOUNTING BOARD AND SEMICONDUCTOR DEVICE COMPOSED THEREOF

PUBN-DATE: April 30, 1996

INVENTOR-INFORMATION:

NAME	COUNTRY
ITO, SEIGO	
SAEGUSA, MASATERU	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOSHIBA MICROELECTRON CORP	
TOSHIBA CORP	

APPL-NO: JP06245238
APPL-DATE: October 11, 1994

INT-CL (IPC): H01L 23/12

ABSTRACT:

PURPOSE: To make uniform the collapse of spherical solders on a BGA package by forming protrusions, having height equal to or lower than that of a plurality of spherical solders, on one side of a package body.

CONSTITUTION: Three protrusions 17A-17C are formed on one side of a package body 11. The protrusions 17A-17C are formed on the periphery of a package body 11 while being spaced apart by a predetermined distance from each other. The protrusion 17A-17C has columnar shape and the height thereof is set equal to or shorter than that of a solder ball 14. Since a BGA package is supported by the protrusions 17A-17C, the solder balls 14 can be collapsed uniformly at all times.

CLAIMS

[Claim(s)]
[Claim 1] BGA package characterized by providing a package mainframe, the LSI chip carried in the aforementioned package mainframe, two or more spherical solder formed in the whole surface side of the aforementioned package mainframe, and the salient which is formed in the whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or has a height lower than it.
[Claim 2] The package substrate characterized by providing the salient which is formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, is formed in order to support the aforementioned BGA package to the two or more electrodes [which two or more spherical solder of BGA package contacts], and whole surface side of the aforementioned substrate mainframe, is the same as that of the height of two or more aforementioned spherical solder, or has a height lower than it.
[Claim 3] BGA package characterized by providing a package mainframe, the LSI chip carried in the aforementioned package mainframe, two or more spherical solder formed in the whole surface side of the aforementioned package mainframe, and at least three pillar-shaped salients which are formed in the whole surface side of the aforementioned package mainframe, are the same as that of the height of two or more aforementioned spherical solder, or have a height lower than it.
[Claim 4] The aforementioned salient is a BGA package according to claim 3 characterized by being formed in the circumference section of the aforementioned package mainframe, respectively.
[Claim 5] The package substrate characterized by providing at least three pillar-shaped salients which are formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, are formed in order to support the aforementioned BGA package to the two or more electrodes [which two or more spherical solder of BGA package contacts], and whole surface side of the aforementioned substrate mainframe, are the same as that of the height of two or more aforementioned spherical solder, or have a height lower than it.
[Claim 6] The aforementioned salient is a package substrate according to claim 5 characterized by being formed in the periphery of two or more aforementioned electrodes, respectively.
[Claim 7] A package mainframe and the LSI chip carried in the aforementioned package mainframe, It is formed in the two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe. BGA package which has 1st at least one salient which is the same as that of the height of two or more aforementioned spherical solder, or has a height lower than it, A substrate mainframe and two or more electrodes which it is formed in the whole surface side of the aforementioned substrate mainframe, and two or more spherical solder of the aforementioned BGA package contacts, It is formed in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe. It is the semiconductor device which is the same as that of the height of two or more aforementioned spherical solder, or possesses the package substrate which has 2nd at least one salient which has a height lower than it, and is characterized by the 1st aforementioned aforementioned salient and the 2nd aforementioned salient not overlapping mutually.
[Claim 8] A package mainframe and the LSI chip carried in the aforementioned package mainframe, It is formed in the two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe. In the half of the height of two or more aforementioned spherical solder, or BGA package which has 1st at least one salient which has a height lower than it, A substrate mainframe and two or more electrodes which it is formed in the whole surface side of the aforementioned substrate mainframe, and two or more spherical solder of the aforementioned BGA package contacts, It is formed in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe. the half of the height of two or more aforementioned spherical solder -- or the semiconductor device characterized by providing the package substrate which has 2nd at least one salient which has a height lower than it, and the 1st aforementioned aforementioned salient and the 2nd aforementioned salient overlapping mutually
[Claim 9] BGA package characterized by providing a package mainframe, the LSI chip carried in the aforementioned package mainframe, two or more spherical solder formed in the whole surface side of the aforementioned package mainframe, and the frame-like salient which is formed so that two or more aforementioned spherical solder may be surrounded in the whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or has a height lower than it.
[Claim 10] The package substrate characterized by to provide the frame-like salient which is formed in the whole-surface side of a substrate mainframe and the aforementioned substrate mainframe, is formed so that two or more electrodes which two or more spherical solder of BGA package contacts, and the electrode of the aforementioned plurality in order to support the aforementioned BGA package to the whole-surface side of the aforementioned substrate mainframe may be surrounded, is the same as that of the height of two or more aforementioned spherical solder, or has a height lower than it.
[Claim 11] BGA package characterized by to provide two linear salients which are formed so that two or more aforementioned spherical solder may be put between the circumference section by the side of a package mainframe, the LSI chip carried in the aforementioned package mainframe, two or more spherical solder formed in the whole surface side of the

aforementioned package mainframe, and the whole surface of the aforementioned package mainframe, are the same as that of the height of two or more aforementioned spherical solder, or have a height lower than it.
[Claim 12] A substrate mainframe and two or more electrodes which it is formed in the whole surface side of the aforementioned substrate mainframe, and two or more spherical solder of BGA package contacts, The package substrate characterized by providing two linear salients which are formed in the whole surface side of the aforementioned substrate mainframe as put two or more aforementioned electrodes in order to support the aforementioned BGA package, are the same as that of the height of two or more aforementioned spherical solder, or have a height lower than it.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the technique of mounting BGA (Ball Grid Array) package in a printed circuit board.
[0002]
[Description of the Prior Art] In recent years, since a surface mount type many-items child LSI package raises the package yield in connection with increase of the number of pins, or advance of the formation of a ** pitch, it changes to QFP (Quad Flat Package) and BGA package is becoming in use.
[0003] This BGA package carries an LSI chip in a package mainframe (wiring substrate), and attaches the spherical solder of the shape of a two-dimensional array in the whole surface side of a package mainframe.
[0004] And according to this BGA package, since spherical solder (terminal) is attached in the whole surface side of a package mainframe two-dimensional, the pitch of a terminal is eased compared with QFP, the package yield improves, and a package cost can be cut down.
[0005]
[Problem(s) to be Solved by the Invention] Drawing 51 shows the status that the conventional BGA package was mounted in the printed circuit board.
[0006] That is, BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more spherical solder 14 arranged at the whole surface side of the package mainframe 11. Moreover, two or more electrodes (terminal) 16 are formed in the whole surface side of a printed circuit board 15.
[0007] However, in case BGA package is mounted in a printed circuit board, the joint of spherical solder 14 and the spherical electrode 16 disappears. For this reason, if time to give heat becomes long, solder 14 comrades which the spherical solder 14 is crushed too much with a self-weight of a package, and adjoin each other will contact, or a position gap will be caused.
[0008] Thus, in case BGA package is conventionally mounted in a printed circuit board, there is a fault which the solder which spherical solder is crushed too much and adjoins contacts, or causes a position gap.
[0009] In case the purpose mounts BGA package in a printed circuit board, as it was made that this invention should solve the above-mentioned fault, and the crushing condition of spherical solder is always kept constant, adjacent solder contacts, or it is made not to cause a position gap.
[0010]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, BGA package of this invention, the package substrate, and the semiconductor device that consists of these have the following configurations, respectively.
[0011] BGA package of this invention is formed in the package mainframe, LSI chip [which is carried in the aforementioned package mainframe], two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the salient which has a height lower than it.

[0012] The package substrate of this invention is formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, it is formed in order to support the aforementioned BGA package to the two or more electrodes [which two or more spherical solder of BGA package contacts], and whole surface side of the aforementioned substrate mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the salient which has a height lower than it.
[0013] BGA package of this invention is formed in the package mainframe, LSI chip [which is carried in the aforementioned package mainframe], two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with at least three pillar-shaped salients which have a height lower than it.
[0014] As for the aforementioned salient, it is good to be formed in the circumference section of the aforementioned package mainframe, respectively.
[0015] The package substrate of this invention is formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, it is formed in order to support the aforementioned BGA package to the two or more electrodes [which two or more spherical solder of BGA package contacts], and whole surface side of the aforementioned substrate mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with at least three pillar-shaped salients which have a height lower than it.
[0016] As for the aforementioned salient, it is good to be formed in the periphery of two or more aforementioned electrodes, respectively.
[0017] The LSI chip by which the semiconductor device of this invention is carried in a package mainframe and the aforementioned package mainframe, It is formed in the two or more spherical solder [which is formed in the whole surface

side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe. It is the same as that of the height of two or more aforementioned spherical solder, or has BGA package which has 1st at least one salient which has a height lower than it. And a substrate mainframe, Two or more electrodes which it is formed in the whole surface side of the aforementioned substrate mainframe, and two or more spherical solder of the aforementioned BGA package contacts, It is formed in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe, and it is the same as that of the height of two or more aforementioned spherical solder, or has the package substrate which has 2nd at least one salient which has a height lower than it, and the 1st aforementioned aforementioned salient and the 2nd aforementioned salient do not overlap mutually.

[0018] The LSI chip by which the semiconductor device of this invention is carried in a package mainframe and the aforementioned package mainframe, It is formed in the two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe. Or it has BGA package which has 1st at least one salient which has a height lower than it. the half of the height of two or more aforementioned spherical solder -- with a substrate mainframe Two or more electrodes which it is formed in the whole surface side of the aforementioned substrate mainframe, and two or more spherical solder of the aforementioned BGA package contacts, it forms in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe -- having -- the half of the height of two or more aforementioned spherical solder -- or it has the package substrate which has 2nd at least one salient which has a height lower than it, and the 1st aforementioned aforementioned salient and the 2nd aforementioned salient overlap mutually

[0019] BGA package of this invention is formed so that two or more aforementioned spherical solder may be surrounded in the package mainframe, LSI chip [which is carried in the aforementioned package mainframe], two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the frame-like salient which has a height lower than it.

[0020] The package substrate of this invention is formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, it is formed so that two or more electrodes which two or more spherical solder of BGA package contacts, and the electrode of the aforementioned plurality in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe may be surrounded, and is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the frame-like salient which has a height lower than it.

[0021] BGA package of this invention is formed so that two or more aforementioned spherical solder may be put between the circumference section by the side of a package mainframe, the LSI chip carried in the aforementioned package mainframe, two or more spherical solder formed in the whole surface side of the aforementioned package mainframe, and the whole surface of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with two linear salients which have a height lower than it.

[0022] The package substrate of this invention is formed in the whole-surface side of a substrate mainframe and the aforementioned substrate mainframe, in order that it may support two or more electrodes which two or more spherical solder of BGA package contacts and aforementioned BGA packages, as it puts two or more aforementioned electrodes, it is formed in the whole-surface side of the aforementioned substrate mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with two linear salients which have a height lower than it.

[0023]

[Function] According to the above-mentioned configuration, the salient is formed at least in one side by the side of the whole surface of BGA package, and the whole surface of a package substrate (side in which spherical solder is formed) (side in which the electrode in contact with spherical solder is formed).

[0024] Moreover, this salient is the same as that of the height of the spherical solder of BGA package, or has the height lower than it.

[0025] therefore, the time of carrying BGA package in a package substrate -- this salient -- ****** -- a sake -- the spherical solder of BGA package -- crushing condition can always be made regularity Moreover, since there is no situation where spherical solder is crushed too much, solder contacts, the package yield does not fall and a low manufacturing cost can be attained.

[0026]

[Example] Hereafter, the semiconductor device which consists of a BGA package of this invention, a package substrate, and these is explained, referring to a drawing.

[0027] [A] Drawing 1 shows the side elevation of BGA package concerning the 1st example of this invention. Moreover, drawing 2 shows the bottom plan view of BGA package of drawing 1 .

[0028] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more spherical solder (henceforth a solder ball) 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.

[0029] Moreover, three salients 17A-17C are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed distance leaves each salients 17A-17C, and they are formed.

[0030] The configuration of these salients 17A-17C is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.

[0031] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A-17C can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A-17C, it is good to make it about 0.5mm.

[0032] It may be made to form salients 17A-17C with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.

[0033] When forming salients 17A-17C in one with the package mainframe 11, salients 17A-17C consist of the same quality

of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A-17C separately [the package mainframe 11], salients 17A-17C can consist of a metal and insulators, such as a resin.
[0034] In addition, the number of salients is not restricted to three pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the circumference section of the package mainframe 11, but may be arranged in the array of the solder ball 14.
[0035] Drawing 3 shows the side elevation of a printed circuit board with which BGA package of the drawing 1 and the drawing 2 is mounted. Moreover, drawing 4 shows the plan of the printed circuit board of drawing 3 .
[0036] The **; lei-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15. Therefore, salients 17A-17C will contact in dashed-line 17A' of the substrate mainframe 15, - 17C', respectively.
[0037] Drawing 5 shows the side elevation of the status that BGA package of the drawing 1 and the drawing 2 was carried in the printed circuit board of the drawing 3 and the drawing 4 .
[0038] That is, since it supports to salients 17A-17C, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0039] According to the above-mentioned configuration, three salients 17A-17C are formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, these salients 17A-17C support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0040] Moreover, if salients 17A-17C are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from a chip 13. Moreover, it is also possible to use salients 17A-17C as a grounding electrode.
[0041] [B] Drawing 6 shows the side elevation of the printed circuit board concerning the 1st example of this invention. Moreover, drawing 7 shows the plan of the printed circuit board of drawing 6 .
[0042] The array-like electrode (terminal) 16 corresponding to the solder ball of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15.
[0043] Moreover, three salients 18A-18C are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A-18C, and they are formed.
[0044] The configuration of these salients 18A-18C is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0045] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A-18C can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A-18C, it is good to make it about 0.5mm.
[0046] It may be made to form salients 18A-18C with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0047] When forming salients 18A-18C in one with the substrate mainframe 15, salients 18A-18C consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A-18C separately [the substrate mainframe 15], salients 18A-18C can consist of a metal and insulators, such as a resin.
[0048] In addition, the number of salients is not restricted to three pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the periphery of the array-like electrode 16, but may be arranged in the array of an electrode 16.
[0049] Drawing 8 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 6 and the drawing 7 . Moreover, drawing 9 shows the bottom plan view of BGA package of drawing 8 .
[0050] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. The solder ball 14 is arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0051] Drawing 10 shows the side elevation of the status that BGA package of the drawing 8 and the drawing 9 was carried in the printed circuit board of the drawing 6 and drawing 7 **.
[0052] That is, since it supports to the salients 18A-18C prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0053] According to the above-mentioned configuration, three salients 18A-18C are formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, these salients 18A-18C support, and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0054] Moreover, if salients 18A-18C are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.
[0055] [C] Drawing 11 shows the side elevation of BGA package concerning the 2nd example of this invention. Moreover, drawing 12 shows the bottom plan view of BGA package of drawing 11 .
[0056] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0057] Moreover, four salients 17A-17D are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed distance leaves each salients 17A-17D, and they are formed. For example, one salients 17A-17D are arranged in each four

corners of the package mainframe 11, respectively.
[0058] The configuration of these salients 17A-17D is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0059] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A-17D can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A-17D, it is good to make it about 0.5mm.
[0060] It may be made to form salients 17A-17D with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0061] When forming salients 17A-17D in one with the package mainframe 11, salients 17A-17D consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A-17D separately [the package mainframe 11], salients 17A-17D can consist of a metal and insulators, such as a resin.
[0062] In addition, the number of salients is not restricted to four pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the circumference section of the package mainframe 11, but may be arranged in the array of the solder ball 14.
[0063] Drawing 13 shows the side elevation of a printed circuit board with which BGA package of the drawing 11 and the drawing 12 is mounted. Moreover, drawing 14 shows the plan of the printed circuit board of drawing 13 .
[0064] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15. Therefore, salients 17A-17D will contact in dashed-line 17A' of the substrate mainframe 15, - 17D', respectively.
[0065] Drawing 15 shows the side elevation of the status that BGA package of the drawing 11 and the drawing 12 was carried in the printed circuit board of the drawing 13 and the drawing 14 .
[0066] That is, since it supports to salients 17A-17D, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0067] According to the above-mentioned configuration, four salients 17A-17D are formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, these salients 17A-17D support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0068] Moreover, if salients 17A-17D are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, it is also possible to use salients 17A-17D as a grounding electrode.
[0069] [D] Drawing 16 shows the side elevation of the printed circuit board concerning the 2nd example of this invention. Moreover, drawing 17 shows the plan of the printed circuit board of drawing 16 .
[0070] The array-like electrode (terminal) 16 corresponding to the solder ball of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15.
[0071] Moreover, four salients 18A-18D are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A-18D, and they are formed. For example, salients 18A-18D are arranged on the diagonal line of the array-like electrode 16, respectively.
[0072] The configuration of these salients 18A-18D is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0073] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A-18D can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A-18D, it is good to make it about 0.5mm.
[0074] It may be made to form salients 18A-18D with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0075] When forming salients 18A-18D in one with the substrate mainframe 15, salients 18A-18D consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A-18D separately [the substrate mainframe 15], salients 18A-18D can consist of a metal and insulators, such as a resin.
[0076] In addition, the number of salients is not restricted to four pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the periphery of the array-like electrode 16, but may be arranged in the array of an electrode 16.
[0077] Drawing 18 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 16 and the drawing 17 . Moreover, drawing 19 shows the bottom plan view of BGA package of drawing 18 .
[0078] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0079] Drawing 20 shows the side elevation of the status that BGA package of the drawing 18 and the drawing 19 was carried in the printed circuit board of the drawing 16 and drawing 17 **.
[0080] That is, since it supports to the salients 18A-18D prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0081] According to the above-mentioned configuration, three salients 18A-18D are formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, these salients 18A-18D support, and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost.

Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0082] Moreover, if salients 18A-18D are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.
[0083] [E] Drawing 21 shows the side elevation of BGA package concerning the 3rd example of this invention. Moreover, drawing 22 shows the bottom plan view of BGA package of drawing 21 .
[0084] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0085] Moreover, two salients 17A and 17B are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed distance leaves each salients 17A and 17B, and they are formed. For example, one salients 17A and 17B are arranged in each two corners on the one diagonal line of the package mainframe 11, respectively.
[0086] The configuration of these salients 17A and 17B is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0087] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A and 17B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A and 17B, it is good to make it about 0.5mm.
[0088] It may be made to form salients 17A and 17B with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0089] When forming salients 17A and 17B in one with the package mainframe 11, salients 17A and 17B consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A and 17B separately [the package mainframe 11], salients 17A and 17B can consist of a metal and insulators, such as a resin.
[0090] Drawing 23 shows the side elevation of the printed circuit board concerning the 3rd example of this invention. Moreover, drawing 24 shows the plan of the printed circuit board of drawing 23 .
[0091] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15.
[0092] In addition, the salients 17A and 17B of BGA package will contact in dashed-line 17A' of a printed circuit board, and 17B', respectively.
[0093] Moreover, two salients 18A and 18B are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A and 18B, and they are formed. For example, one salients 18A and 18B are arranged on [each] the one diagonal line of the array-like electrode 16, respectively.
[0094] The configuration of these salients 18A and 18B is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0095] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A and 18B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A and 18B, it is good to make it about 0.5mm.
[0096] It may be made to form salients 18A and 18B with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0097] When forming salients 18A and 18B in one with the substrate mainframe 15, salients 18A and 18B consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A and 18B separately [the substrate mainframe 15], salients 18A and 18B can consist of a metal and insulators, such as a resin.
[0098] Drawing 25 shows the side elevation of the status that BGA package of the drawing 21 and the drawing 22 was carried in the printed circuit board of the drawing 23 and the drawing 24 .
[0099] that is, since BGA package is looked like [the salients 17A and 17B and the salients 18A and 18B of a printed circuit board] and it supports, it does not have that the crushing condition of the solder ball 14 is always fixed, and the situation where become and the solder ball 14 is crushed too much
[0100] In addition, a salient of BGA package and a salient of a printed circuit board are arranged so that it may not overlap mutually.
[0101] According to the above-mentioned configuration, the height is formed in the rear-face [of BGA package], and printed-circuit-board side, respectively. For this reason, these salients 17A, 17B, 18A, and 18B support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0102] Moreover, if salients 17A, 17B, 18A, and 18B are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, about salients 17A and 17B, using as a grounding electrode is also possible.
[0103] [F] Drawing 26 shows the side elevation of BGA package concerning the 4th example of this invention. Moreover, drawing 27 shows the bottom plan view of BGA package of drawing 26 .
[0104] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0105] Moreover, three salients 17A-17C are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed

distance leaves each salients 17A-17C, and they are formed.
[0106] the configuration of these salients 17A-17C is pillar-shaped (the shape of for example, a prism) -- it is -- the height -- the half of the height (diameter) of the solder ball 14 -- or it is set up so that it may become lower than it
[0107] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, as for the height of salients 17A-17C, it is good to make it about 0.3mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A-17C, it is good to make it about 0.25mm.
[0108] It may be made to form salients 17A-17C with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0109] When forming salients 17A-17C in one with the package mainframe 11, salients 17A-17C consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A-17C separately [the package mainframe 11], salients 17A-17C can consist of a metal and insulators, such as a resin.
[0110] Drawing 28 shows the side elevation of the printed circuit board concerning the 4th example of this invention. Moreover, drawing 29 shows the plan of the printed circuit board of drawing 28 .
[0111] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of a printed circuit board.
[0112] Moreover, three salients 18A-18C are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A-18C, and they are formed.
[0113] the configuration of these salients 18A-18C is pillar-shaped (the shape of for example, a prism) -- it is -- the height -- the half of the height (diameter) of the solder ball of BGA package -- or it is set up so that it may become lower than it
[0114] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, as for the height of salients 18A-18C, it is good to make it about 0.3mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A-18C, it is good to make it about 0.25mm.
[0115] It may be made to form salients 18A-18C with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0116] When forming salients 18A-18C in one with the substrate mainframe 15, salients 18A-18C consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A-18C separately [the substrate mainframe 15], salients 18A-18C can consist of a metal and insulators, such as a resin.
[0117] Drawing 30 shows the side elevation of the status that BGA package of the drawing 26 and the drawing 27 was carried in the printed circuit board of the drawing 28 and the drawing 29 .
[0118] that is, since it boils and supports to the salients 17A-17C and the heights 18A-18C of a printed circuit board, BGA package does not have that the crushing condition of the solder ball 14 is always fixed, and the situation where become and the solder ball 14 is crushed too much
[0119] In addition, the salient of BGA package and the salient of a printed circuit board are arranged so that it may overlap mutually.
[0120] According to the above-mentioned configuration, the salient is formed in the rear-face [of BGA package], and printed-circuit-board side, respectively. For this reason, these salients 17A-17C, and 18A-18C support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0121] Moreover, a printed circuit board can also be made to emit the heat which will generate them from LSI chip 13 if salients 17A-17C, and 18A-18C are constituted from a material which has low thermal resistance.
[0122] [G] Drawing 31 shows the side elevation of BGA package concerning the 5th example of this invention. Moreover, drawing 32 shows the bottom plan view of BGA package of drawing 31 .
[0123] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0124] Moreover, the frame-like salient 17 is formed in the whole surface side of the package mainframe 11. Salient 17 is formed in the circumference section of the package mainframe 11, and as it encloses the solder ball 14, it is formed.
[0125] The height of this salient 17 is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0126] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salient 17 can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salient 17, it is good to make it about 0.5mm.
[0127] It may be made to form salient 17 with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0128] When forming salient 17 in one with the package mainframe 11, salient 17 consists of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salient 17 separately [the package mainframe 11], salient 17 can consist of a metal and insulators, such as a resin.
[0129] Drawing 33 shows the side elevation of a printed circuit board with which BGA package of the drawing 31 and the drawing 32 is mounted. Moreover, drawing 34 shows the plan of the printed circuit board of drawing 33 .
[0130] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of a printed circuit board. Therefore, salient 17 will contact in dashed-line 17' of a printed circuit board, respectively.
[0131] Drawing 35 shows the side elevation of the status that BGA package of the drawing 31 and the drawing 32 was carried in the printed circuit board of the drawing 33 and the drawing 34 .
[0132] That is, since it supports to the salient 17, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.

[0133] According to the above-mentioned configuration, the frame-like salient 17 is formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, this salient 17 supports and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0134] Moreover, if salient 17 is constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, it is also possible to use salient 17 as a grounding electrode.
[0135] [H] Drawing 36 shows the side elevation of the package substrate concerning the 5th example of this invention. Moreover, drawing 37 shows the plan of the package substrate of drawing 36 .
[0136] The electrode (terminal) 16 is formed in the whole surface side of the substrate mainframe 15 in the shape of corresponding to the solder ball of BGA package] an array. In addition, BGA package is arranged in dashed-line X of a printed circuit board.
[0137] Moreover, the frame-like salient 18 is formed in the whole surface side of the substrate mainframe 15. Salient 18 is formed in the periphery of the array-like electrode 16, and as it encloses the array-like electrode 16, it is formed.
[0138] The height of this salient 18 is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0139] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salient 18 can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salient 18, it is good to make it about 0.5mm.
[0140] It may be made to form salient 18 with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0141] When forming salient 18 in one with the substrate mainframe 15, salient 18 consists of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salient 18 separately [the substrate mainframe 15], salient 18 can consist of a metal and insulators, such as a resin.
[0142] Drawing 38 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 36 and the drawing 37 . Moreover, drawing 39 shows the bottom plan view of BGA package of drawing 38 .
[0143] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0144] Drawing 40 shows the side elevation of the status that BGA package of the drawing 38 and the drawing 39 was carried in the printed circuit board of the drawing 36 and drawing 37 **.
[0145] That is, since it supports to the salient 18 prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0146] According to the above-mentioned configuration, the frame-like salient 18 is formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, this salient 18 supports and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0147] Moreover, if salient 18 is constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.
[0148] [I] View 41 shows the side elevation of BGA package concerning the 6th example of this invention. Moreover, drawing 42 shows the bottom plan view of BGA package of drawing 41 .
[0149] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0150] Moreover, salients 17A and 17B are formed in the whole surface side of the package mainframe 11. Each salients 17A and 17B are formed in the circumference section of the package mainframe 11, respectively, and are formed in the line. For example, one salients 17A and 17B are arranged in each side where the package mainframe 11 counters, respectively.
[0151] The height of these salients 17A and 17B is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0152] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A and 17B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A and 17B, it is good to make it about 0.5mm.
[0153] It may be made to form salients 17A and 17B with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0154] When forming salients 17A and 17B in one with the package mainframe 11, salients 17A and 17B consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A and 17B separately [the package mainframe 11], salients 17A and 17B can consist of a metal and insulators, such as a resin.
[0155] Drawing 43 shows the side elevation of a printed circuit board with which BGA package of the drawing 41 and the drawing 42 is mounted. Moreover, drawing 44 shows the plan of the printed circuit board of drawing 43 .
[0156] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of a printed circuit board. Therefore, salients 17A and 17B will contact in dashed-line 17A' of a printed circuit board, and 17B', respectively.
[0157] Drawing 45 shows the side elevation of the status that BGA package of the drawing 41 and the drawing 42 was carried in the printed circuit board of the drawing 43 and the drawing 44 .
[0158] That is, since it supports to salients 17A and 17B, the crushing condition of the solder ball 14 becomes always fixed,

and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0159] According to the above-mentioned configuration, the linear salients 17A and 17B are formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, these salients 17A and 17B support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0160] Moreover, if salients 17A and 17B are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, it is also possible to use salients 17A and 17B as a grounding electrode.
[0161] [J] Drawing 46 shows the side elevation of the package substrate concerning the 6th example of this invention. Moreover, drawing 47 shows the plan of the package substrate of drawing 46 .
[0162] The electrode (terminal) 16 is formed in the whole surface side of the substrate mainframe 15 in the shape of corresponding to the solder ball of BGA package] an array. In addition, BGA package is arranged in dashed-line X of a printed circuit board.
[0163] Moreover, salients 18A and 18B are formed in the whole surface side of the substrate mainframe 15. Each salients 18A and 18B are formed so that it may be formed in the periphery of the array-like electrode 16 and it may become a line. For example, it counters, respectively and salients 18A and 18B are arranged so that the array-like electrode 16 may be put in between.
[0164] The height of these salients 18A and 18B is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0165] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A and 18B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A and 18B, it is good to make it about 0.5mm.
[0166] It may be made to form salients 18A and 18B with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0167] When forming salients 18A and 18B in one with the substrate mainframe 15, salients 18A and 18B consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A and 18B separately [the substrate mainframe 15], salients 18A and 18B can consist of a metal and insulators, such as a resin.
[0168] Drawing 48 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 46 and the drawing 47 . Moreover, drawing 49 shows the bottom plan view of BGA package of drawing 48 .
[0169] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0170] Drawing 50 shows the side elevation of the status that BGA package of the drawing 48 and the drawing 49 was carried in the printed circuit board of the drawing 46 and drawing 47 **.
[0171] That is, since it supports to the salients 18A and 18B prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0172] According to the above-mentioned configuration, the linear salients 18A and 18B are formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, these salients 18A and 18B support, and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0173] Moreover, if salients 18A and 18B are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.
[0174]
[Effect of the Invention] As mentioned above, according to BGA package of this invention, a package substrate, and the semiconductor device that consists of these, the following effects are done so as explained.
[0175] The height is formed at least in one side by the side of the rear face of BGA package, and the whole surface of a printed circuit board (side in which a solder ball is formed) (side in which the electrode in contact with a solder ball is formed).
[0176] therefore, the time of carrying BGA package in a printed circuit board -- this salient -- ****** -- a sake -- BGA package -- crushing condition of a solder ball can always be made regularity
[0177] That is, since there is no situation where the solder ball of BGA package is crushed too much, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0178] Moreover, if this salient is constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from a chip.
[0179] Furthermore, when a salient is formed in BGA package side, it is also possible to use this salient as a grounding electrode.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

Field

[Field of the Invention] Especially this invention relates to the technique of mounting BGA (Ball Grid Array) package in a printed circuit board.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

Technique

[Description of the Prior Art] In recent years, since a surface mount type many-items child LSI package raises the package yield in connection with increase of the number of pins, or advance of the formation of a ** pitch, it changes to QFP (Quad Flat Package) and BGA package is becoming in use.
[0003] This BGA package carries an LSI chip in a package mainframe (wiring substrate), and attaches the spherical solder of the shape of a two-dimensional array in the whole surface side of a package mainframe.
[0004] And according to this BGA package, since spherical solder (terminal) is attached in the whole surface side of a package mainframe two-dimensional, the pitch of a terminal is eased compared with QFP, the package yield improves, and a package cost can be cut down.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

Effect

[Effect of the Invention] As mentioned above, according to BGA package of this invention, a package substrate, and the semiconductor device that consists of these, the following effects are done so as explained.
[0175] The height is formed at least in one side by the side of the rear face of BGA package, and the whole surface of a printed circuit board (side in which a solder ball is formed) (side in which the electrode in contact with a solder ball is formed).
[0176] therefore, the time of carrying BGA package in a printed circuit board -- this salient -- ****** -- a sake -- BGA package -- crushing condition of a solder ball can always be made regularity
[0177] That is, since there is no situation where the solder ball of BGA package is crushed too much, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0178] Moreover, if this salient is constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from a chip.
[0179] Furthermore, when a salient is formed in BGA package side, it is also possible to use this salient as a grounding electrode.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Drawing 51 shows the status that the conventional BGA package was mounted in the printed circuit board.
[0006] That is, BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more spherical solder 14 arranged at the whole surface side of the package mainframe 11. Moreover, two or more electrodes (terminal) 16 are formed in the whole surface side of a printed circuit board 15.
[0007] However, in case BGA package is mounted in a printed circuit board, the joint of spherical solder 14 and the spherical electrode 16 disappears. For this reason, if time to give heat becomes long, solder 14 comrades which the spherical solder 14 is crushed too much with a self-weight of a package, and adjoin each other will contact, or a position gap will be caused.
[0008] Thus, in case BGA package is conventionally mounted in a printed circuit board, there is a fault which the solder which spherical solder is crushed too much and adjoins contacts, or causes a position gap.
[0009] In case the purpose mounts BGA package in a printed circuit board, as it was made that this invention should solve the above-mentioned fault, and the crushing condition of spherical solder is always kept constant, adjacent solder contacts, or it is made not to cause a position gap.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to attain the above-mentioned purpose, BGA package of this invention, the package substrate, and the semiconductor device that consists of these have the following configurations, respectively.
[0011] BGA package of this invention is formed in the package mainframe, LSI chip [which is carried in the aforementioned package mainframe], two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the salient which has a height lower than it.

[0012] The package substrate of this invention is formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, it is formed in order to support the aforementioned BGA package to the two or more electrodes [which two or more spherical solder of BGA package contacts], and whole surface side of the aforementioned substrate mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the salient which has a height lower than it.
[0013] BGA package of this invention is formed in the package mainframe, LSI chip [which is carried in the aforementioned package mainframe], two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with at least three pillar-shaped salients which have a height lower than it.
[0014] As for the aforementioned salient, it is good to be formed in the circumference section of the aforementioned package mainframe, respectively.
[0015] The package substrate of this invention is formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, it is formed in order to support the aforementioned BGA package to the two or more electrodes [which two or more spherical solder of BGA package contacts], and whole surface side of the aforementioned substrate mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with at least three pillar-shaped salients which have a height lower than it.
[0016] As for the aforementioned salient, it is good to be formed in the periphery of two or more aforementioned electrodes, respectively.
[0017] The LSI chip by which the semiconductor device of this invention is carried in a package mainframe and the aforementioned package mainframe, It is formed in the two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe. It is the same as that of the height of two or more aforementioned spherical solder, or has BGA package which has 1st at least one salient which has a height lower than it. And a substrate mainframe, Two or more electrodes which it is formed in the whole surface side of the aforementioned substrate mainframe, and two or more spherical solder of the aforementioned BGA package contacts, It is formed in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe, and it is the same as that of the height of two or more aforementioned spherical solder, or has the package substrate which has 2nd at least one salient which has a height lower than it, and the 1st aforementioned aforementioned salient and the 2nd aforementioned salient do not overlap mutually.
[0018] The LSI chip by which the semiconductor device of this invention is carried in a package mainframe and the aforementioned package mainframe, It is formed in the two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe. Or it has BGA package which has 1st at least one salient which has a height lower than it. the half of the height of two or more aforementioned spherical solder -- with a substrate mainframe Two or more electrodes which it is formed in the whole surface side of the aforementioned substrate mainframe, and two or more spherical solder of the aforementioned BGA package contacts, it forms in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe -- having -- the half of the height of two or more aforementioned spherical solder -- or it has the package substrate which has 2nd at least one salient which has a height lower than it, and the 1st aforementioned aforementioned salient and the 2nd aforementioned salient overlap mutually
[0019] BGA package of this invention is formed so that two or more aforementioned spherical solder may be surrounded in the package mainframe, LSI chip [which is carried in the aforementioned package mainframe], two or more spherical solder [which is formed in the whole surface side of the aforementioned package mainframe], and whole surface side of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the frame-like salient which has a height lower than it.
[0020] The package substrate of this invention is formed in the whole surface side of a substrate mainframe and the aforementioned substrate mainframe, it is formed so that two or more electrodes which two or more spherical solder of BGA package contacts, and the electrode of the aforementioned plurality in order to support the aforementioned BGA package to the whole surface side of the aforementioned substrate mainframe may be surrounded, and is the same as that of the height of two or more aforementioned spherical solder, or is equipped with the frame-like salient which has a height lower than it.
[0021] BGA package of this invention is formed so that two or more aforementioned spherical solder may be put between

the circumference section by the side of a package mainframe, the LSI chip carried in the aforementioned package mainframe, two or more spherical solder formed in the whole surface side of the aforementioned package mainframe, and the whole surface of the aforementioned package mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with two linear salients which have a height lower than it.

[0022] The package substrate of this invention is formed in the whole-surface side of a substrate mainframe and the aforementioned substrate mainframe, in order that it may support two or more electrodes which two or more spherical solder of BGA package contacts and aforementioned BGA packages, as it puts two or more aforementioned electrodes, it is formed in the whole-surface side of the aforementioned substrate mainframe, is the same as that of the height of two or more aforementioned spherical solder, or is equipped with two linear salients which have a height lower than it.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

OPERATION

[Function] According to the above-mentioned configuration, the salient is formed at least in one side by the side of the whole surface of BGA package, and the whole surface of a package substrate (side in which spherical solder is formed) (side in which the electrode in contact with spherical solder is formed).
[0024] Moreover, this salient is the same as that of the height of the spherical solder of BGA package, or has the height lower than it.
[0025] therefore, the time of carrying BGA package in a package substrate -- this salient -- ****** -- a sake -- the spherical solder of BGA package -- crushing condition can always be made regularity Moreover, since there is no situation where spherical solder is crushed too much, solder contacts, the package yield does not fall and a low manufacturing cost can be attained.

[Translation done.]

EXAMPLE

[Example] Hereafter, the semiconductor device which consists of a BGA package of this invention, a package substrate, and these is explained, referring to a drawing.
[0027] [A] Drawing 1 shows the side elevation of BGA package concerning the 1st example of this invention. Moreover, drawing 2 shows the bottom plan view of BGA package of drawing 1 .
[0028] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more spherical solder (henceforth a solder ball) 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0029] Moreover, three salients 17A-17C are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed distance leaves each salients 17A-17C, and they are formed.
[0030] The configuration of these salients 17A-17C is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0031] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A-17C can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A-17C, it is good to make it about 0.5mm.
[0032] It may be made to form salients 17A-17C with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0033] When forming salients 17A-17C in one with the package mainframe 11, salients 17A-17C consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A-17C separately [the package mainframe 11], salients 17A-17C can consist of a metal and insulators, such as a resin.
[0034] In addition, the number of salients is not restricted to three pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the circumference section of the package mainframe 11, but may be arranged in the array of the solder ball 14.
[0035] Drawing 3 shows the side elevation of a printed circuit board with which BGA package of the drawing 1 and the drawing 2 is mounted. Moreover, drawing 4 shows the plan of the printed circuit board of drawing 3 .
[0036] The **; lei-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15. Therefore, salients 17A-17C will contact in dashed-line 17A' of the substrate mainframe 15, - 17C', respectively.
[0037] Drawing 5 shows the side elevation of the status that BGA package of the drawing 1 and the drawing 2 was carried in the printed circuit board of the drawing 3 and the drawing 4 .
[0038] That is, since it supports to salients 17A-17C, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0039] According to the above-mentioned configuration, three salients 17A-17C are formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, these salients 17A-17C support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0040] Moreover, if salients 17A-17C are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from a chip 13. Moreover, it is also possible to use salients 17A-17C as a grounding electrode.
[0041] [B] Drawing 6 shows the side elevation of the printed circuit board concerning the 1st example of this invention. Moreover, drawing 7 shows the plan of the printed circuit board of drawing 6 .
[0042] The array-like electrode (terminal) 16 corresponding to the solder ball of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15.
[0043] Moreover, three salients 18A-18C are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A-18C, and they are formed.
[0044] The configuration of these salients 18A-18C is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0045] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A-18C can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A-18C, it is good to make it about 0.5mm.
[0046] It may be made to form salients 18A-18C with the substrate mainframe 15 in one, or may be made to form the

substrate mainframe 15 separately.
[0047] When forming salients 18A-18C in one with the substrate mainframe 15, salients 18A-18C consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A-18C separately [the substrate mainframe 15], salients 18A-18C can consist of a metal and insulators, such as a resin.
[0048] In addition, the number of salients is not restricted to three pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the periphery of the array-like electrode 16, but may be arranged in the array of an electrode 16.
[0049] Drawing 8 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 6 and the drawing 7 . Moreover, drawing 9 shows the bottom plan view of BGA package of drawing 8 .
[0050] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. The solder ball 14 is arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0051] Drawing 10 shows the side elevation of the status that BGA package of the drawing 8 and the drawing 9 was carried in the printed circuit board of the drawing 6 and drawing 7 **.
[0052] That is, since it supports to the salients 18A-18C prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0053] According to the above-mentioned configuration, three salients 18A-18C are formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, these salients 18A-18C support, and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0054] Moreover, if salients 18A-18C are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.
[0055] [C] Drawing 11 shows the side elevation of BGA package concerning the 2nd example of this invention. Moreover, drawing 12 shows the bottom plan view of BGA package of drawing 11 .
[0056] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0057] Moreover, four salients 17A-17D are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed distance leaves each salients 17A-17D, and they are formed. For example, one salients 17A-17D are arranged in each four corners of the package mainframe 11, respectively.
[0058] The configuration of these salients 17A-17D is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0059] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A-17D can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A-17D, it is good to make it about 0.5mm.
[0060] It may be made to form salients 17A-17D with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0061] When forming salients 17A-17D in one with the package mainframe 11, salients 17A-17D consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A-17D separately [the package mainframe 11], salients 17A-17D can consist of a metal and insulators, such as a resin.
[0062] In addition, the number of salients is not restricted to four pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the circumference section of the package mainframe 11, but may be arranged in the array of the solder ball 14.
[0063] Drawing 13 shows the side elevation of a printed circuit board with which BGA package of the drawing 11 and the drawing 12 is mounted. Moreover, drawing 14 shows the plan of the printed circuit board of drawing 13 .
[0064] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15. Therefore, salients 17A-17D will contact in dashed-line 17A' of the substrate mainframe 15, - 17D', respectively.
[0065] Drawing 15 shows the side elevation of the status that BGA package of the drawing 11 and the drawing 12 was carried in the printed circuit board of the drawing 13 and the drawing 14 .
[0066] That is, since it supports to salients 17A-17D, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0067] According to the above-mentioned configuration, four salients 17A-17D are formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, these salients 17A-17D support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0068] Moreover, if salients 17A-17D are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, it is also possible to use salients 17A-17D as a grounding electrode.
[0069] [D] Drawing 16 shows the side elevation of the printed circuit board concerning the 2nd example of this invention. Moreover, drawing 17 shows the plan of the printed circuit board of drawing 16 .
[0070] The array-like electrode (terminal) 16 corresponding to the solder ball of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15.

[0071] Moreover, four salients 18A-18D are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A-18D, and they are formed. For example, salients 18A-18D are arranged on the diagonal line of the array-like electrode 16, respectively.
[0072] The configuration of these salients 18A-18D is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0073] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A-18D can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A-18D, it is good to make it about 0.5mm.
[0074] It may be made to form salients 18A-18D with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0075] When forming salients 18A-18D in one with the substrate mainframe 15, salients 18A-18D consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A-18D separately [the substrate mainframe 15], salients 18A-18D can consist of a metal and insulators, such as a resin.
[0076] In addition, the number of salients is not restricted to four pieces, and like this example, when a salient is pillar-shaped, it should just be three or more pieces. Moreover, the position of a salient is not restricted to the periphery of the array-like electrode 16, but may be arranged in the array of an electrode 16.
[0077] Drawing 18 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 16 and the drawing 17 . Moreover, drawing 19 shows the bottom plan view of BGA package of drawing 18 .
[0078] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0079] Drawing 20 shows the side elevation of the status that BGA package of the drawing 18 and the drawing 19 was carried in the printed circuit board of the drawing 16 and drawing 17 **.
[0080] That is, since it supports to the salients 18A-18D prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0081] According to the above-mentioned configuration, three salients 18A-18D are formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, these salients 18A-18D support, and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0082] Moreover, if salients 18A-18D are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.
[0083] [E] Drawing 21 shows the side elevation of BGA package concerning the 3rd example of this invention. Moreover, drawing 22 shows the bottom plan view of BGA package of drawing 21 .
[0084] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0085] Moreover, two salients 17A and 17B are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed distance leaves each salients 17A and 17B, and they are formed. For example, one salients 17A and 17B are arranged in each two corners on the one diagonal line of the package mainframe 11, respectively.
[0086] The configuration of these salients 17A and 17B is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0087] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A and 17B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A and 17B, it is good to make it about 0.5mm.
[0088] It may be made to form salients 17A and 17B with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0089] When forming salients 17A and 17B in one with the package mainframe 11, salients 17A and 17B consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A and 17B separately [the package mainframe 11], salients 17A and 17B can consist of a metal and insulators, such as a resin.
[0090] Drawing 23 shows the side elevation of the printed circuit board concerning the 3rd example of this invention. Moreover, drawing 24 shows the plan of the printed circuit board of drawing 23 .
[0091] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of the substrate mainframe 15.
[0092] In addition, the salients 17A and 17B of BGA package will contact in dashed-line 17A' of a printed circuit board, and 17B', respectively.
[0093] Moreover, two salients 18A and 18B are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A and 18B, and they are formed. For example, one salients 18A and 18B are arranged on [each] the one diagonal line of the array-like electrode 16, respectively.
[0094] The configuration of these salients 18A and 18B is pillar-shaped (the shape of for example, a prism), the height is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.

[0095] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A and 18B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A and 18B, it is good to make it about 0.5mm.
[0096] It may be made to form salients 18A and 18B with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0097] When forming salients 18A and 18B in one with the substrate mainframe 15, salients 18A and 18B consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A and 18B separately [the substrate mainframe 15], salients 18A and 18B can consist of a metal and insulators, such as a resin.
[0098] Drawing 25 shows the side elevation of the status that BGA package of the drawing 21 and the drawing 22 was carried in the printed circuit board of the drawing 23 and the drawing 24 .
[0099] that is, since BGA package is looked like [the salients 17A and 17B and the salients 18A and 18B of a printed circuit board] and it supports, it does not have that the crushing condition of the solder ball 14 is always fixed, and the situation where become and the solder ball 14 is crushed too much
[0100] In addition, a salient of BGA package and a salient of a printed circuit board are arranged so that it may not overlap mutually.
[0101] According to the above-mentioned configuration, the height is formed in the rear-face [of BGA package], and printed-circuit-board side, respectively. For this reason, these salients 17A, 17B, 18A, and 18B support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0102] Moreover, if salients 17A, 17B, 18A, and 18B are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, about salients 17A and 17B, using as a grounding electrode is also possible.
[0103] [F] Drawing 26 shows the side elevation of BGA package concerning the 4th example of this invention. Moreover, drawing 27 shows the bottom plan view of BGA package of drawing 26 .
[0104] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0105] Moreover, three salients 17A-17C are formed in the whole surface side of the package mainframe 11. Without being formed in the circumference section of the package mainframe 11, and being collected into one place, mutually, only fixed distance leaves each salients 17A-17C, and they are formed.
[0106] the configuration of these salients 17A-17C is pillar-shaped (the shape of for example, a prism) -- it is -- the height -- the half of the height (diameter) of the solder ball 14 -- or it is set up so that it may become lower than it
[0107] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, as for the height of salients 17A-17C, it is good to make it about 0.3mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A-17C, it is good to make it about 0.25mm.
[0108] It may be made to form salients 17A-17C with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0109] When forming salients 17A-17C in one with the package mainframe 11, salients 17A-17C consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A-17C separately [the package mainframe 11], salients 17A-17C can consist of a metal and insulators, such as a resin.
[0110] Drawing 28 shows the side elevation of the printed circuit board concerning the 4th example of this invention. Moreover, drawing 29 shows the plan of the printed circuit board of drawing 28 .
[0111] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of a printed circuit board.
[0112] Moreover, three salients 18A-18C are formed in the whole surface side of the substrate mainframe 15. Without being formed in the periphery of the array-like electrode 16, and being collected into one place, mutually, only fixed distance leaves each salients 18A-18C, and they are formed.
[0113] the configuration of these salients 18A-18C is pillar-shaped (the shape of for example, a prism) -- it is -- the height -- the half of the height (diameter) of the solder ball of BGA package -- or it is set up so that it may become lower than it
[0114] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, as for the height of salients 18A-18C, it is good to make it about 0.3mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A-18C, it is good to make it about 0.25mm.
[0115] It may be made to form salients 18A-18C with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0116] When forming salients 18A-18C in one with the substrate mainframe 15, salients 18A-18C consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A-18C separately [the substrate mainframe 15], salients 18A-18C can consist of a metal and insulators, such as a resin.
[0117] Drawing 30 shows the side elevation of the status that BGA package of the drawing 26 and the drawing 27 was carried in the printed circuit board of the drawing 28 and the drawing 29 .
[0118] that is, since it boils and supports to the salients 17A-17C and the heights 18A-18C of a printed circuit board, BGA package does not have that the crushing condition of the solder ball 14 is always fixed, and the situation where become and the solder ball 14 is crushed too much
[0119] In addition, the salient of BGA package and the salient of a printed circuit board are arranged so that it may overlap mutually.
[0120] According to the above-mentioned configuration, the salient is formed in the rear-face [of BGA package], and printed-circuit-board side, respectively. For this reason, these salients 17A-17C, and 18A-18C support, and the situation

where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0121] Moreover, a printed circuit board can also be made to emit the heat which will generate them from LSI chip 13 if salients 17A-17C, and 18A-18C are constituted from a material which has low thermal resistance.
[0122] [G] Drawing 31 shows the side elevation of BGA package concerning the 5th example of this invention. Moreover, drawing 32 shows the bottom plan view of BGA package of drawing 31 .
[0123] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0124] Moreover, the frame-like salient 17 is formed in the whole surface side of the package mainframe 11. Salient 17 is formed in the circumference section of the package mainframe 11, and as it encloses the solder ball 14, it is formed.
[0125] The height of this salient 17 is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0126] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salient 17 can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salient 17, it is good to make it about 0.5mm.
[0127] It may be made to form salient 17 with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0128] When forming salient 17 in one with the package mainframe 11, salient 17 consists of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salient 17 separately [the package mainframe 11], salient 17 can consist of a metal and insulators, such as a resin.
[0129] Drawing 33 shows the side elevation of a printed circuit board with which BGA package of the drawing 31 and the drawing 32 is mounted. Moreover, drawing 34 shows the plan of the printed circuit board of drawing 33 .
[0130] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of a printed circuit board. Therefore, salient 17 will contact in dashed-line 17' of a printed circuit board, respectively.
[0131] Drawing 35 shows the side elevation of the status that BGA package of the drawing 31 and the drawing 32 was carried in the printed circuit board of the drawing 33 and the drawing 34 .
[0132] That is, since it supports to the salient 17, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0133] According to the above-mentioned configuration, the frame-like salient 17 is formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, this salient 17 supports and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0134] Moreover, if salient 17 is constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, it is also possible to use salient 17 as a grounding electrode.
[0135] [H] Drawing 36 shows the side elevation of the package substrate concerning the 5th example of this invention. Moreover, drawing 37 shows the plan of the package substrate of drawing 36 .
[0136] The electrode (terminal) 16 is formed in the whole surface side of the substrate mainframe 15 in the shape of corresponding to the solder ball of BGA package] an array. In addition, BGA package is arranged in dashed-line X of a printed circuit board.
[0137] Moreover, the frame-like salient 18 is formed in the whole surface side of the substrate mainframe 15. Salient 18 is formed in the periphery of the array-like electrode 16, and as it encloses the array-like electrode 16, it is formed.
[0138] The height of this salient 18 is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0139] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salient 18 can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salient 18, it is good to make it about 0.5mm.
[0140] It may be made to form salient 18 with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0141] When forming salient 18 in one with the substrate mainframe 15, salient 18 consists of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salient 18 separately [the substrate mainframe 15], salient 18 can consist of a metal and insulators, such as a resin.
[0142] Drawing 38 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 36 and the drawing 37 . Moreover, drawing 39 shows the bottom plan view of BGA package of drawing 38 .
[0143] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0144] Drawing 40 shows the side elevation of the status that BGA package of the drawing 38 and the drawing 39 was carried in the printed circuit board of the drawing 36 and drawing 37 **.
[0145] That is, since it supports to the salient 18 prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0146] According to the above-mentioned configuration, the frame-like salient 18 is formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, this salient 18 supports

and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0147] Moreover, if salient 18 is constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.
[0148] [I] View 41 shows the side elevation of BGA package concerning the 6th example of this invention. Moreover, drawing 42 shows the bottom plan view of BGA package of drawing 41 .
[0149] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0150] Moreover, salients 17A and 17B are formed in the whole surface side of the package mainframe 11. Each salients 17A and 17B are formed in the circumference section of the package mainframe 11, respectively, and are formed in the line. For example, one salients 17A and 17B are arranged in each side where the package mainframe 11 counters, respectively.
[0151] The height of these salients 17A and 17B is the same as the height (diameter) of the solder ball 14, or it is set up so that it may become lower than it.
[0152] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 17A and 17B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 17A and 17B, it is good to make it about 0.5mm.
[0153] It may be made to form salients 17A and 17B with the package mainframe 11 in one, or may be made to form the package mainframe 11 separately.
[0154] When forming salients 17A and 17B in one with the package mainframe 11, salients 17A and 17B consist of the same quality of the material (for example, glass epoxy) as the package mainframe 11. Moreover, when forming salients 17A and 17B separately [the package mainframe 11], salients 17A and 17B can consist of a metal and insulators, such as a resin.
[0155] Drawing 43 shows the side elevation of a printed circuit board with which BGA package of the drawing 41 and the drawing 42 is mounted. Moreover, drawing 44 shows the plan of the printed circuit board of drawing 43 .
[0156] The array-like electrode (terminal) 16 corresponding to the solder ball 14 of BGA package is formed in the whole surface side of the substrate mainframe 15. In addition, BGA package is arranged in dashed-line X of a printed circuit board. Therefore, salients 17A and 17B will contact in dashed-line 17A' of a printed circuit board, and 17B', respectively.
[0157] Drawing 45 shows the side elevation of the status that BGA package of the drawing 41 and the drawing 42 was carried in the printed circuit board of the drawing 43 and the drawing 44 .
[0158] That is, since it supports to salients 17A and 17B, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0159] According to the above-mentioned configuration, the linear salients 17A and 17B are formed in the rear-face side (side in which a solder ball is formed) of BGA package. For this reason, these salients 17A and 17B support, and the situation where a next door and the solder ball 14 are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0160] Moreover, if salients 17A and 17B are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13. Moreover, it is also possible to use salients 17A and 17B as a grounding electrode.
[0161] [J] Drawing 46 shows the side elevation of the package substrate concerning the 6th example of this invention. Moreover, drawing 47 shows the plan of the package substrate of drawing 46 .
[0162] The electrode (terminal) 16 is formed in the whole surface side of the substrate mainframe 15 in the shape of corresponding to the solder ball of BGA package] an array. In addition, BGA package is arranged in dashed-line X of a printed circuit board.
[0163] Moreover, salients 18A and 18B are formed in the whole surface side of the substrate mainframe 15. Each salients 18A and 18B are formed so that it may be formed in the periphery of the array-like electrode 16 and it may become a line. For example, it counters, respectively and salients 18A and 18B are arranged so that the array-like electrode 16 may be put in between.
[0164] The height of these salients 18A and 18B is the same as the height (diameter) of the solder ball of BGA package, or it is set up so that it may become lower than it.
[0165] Specifically, when the diameter of the solder ball 14 is about 0.75mm and a pitch is about 1.5mm, the height of salients 18A and 18B can also ensure a package while it can prevent a contact of solder balls most effectively, if it is made into about 0.6mm. Moreover, when the diameter of the solder ball 14 is about 0.6mm and a pitch is about 1.0mm, as for the height of salients 18A and 18B, it is good to make it about 0.5mm.
[0166] It may be made to form salients 18A and 18B with the substrate mainframe 15 in one, or may be made to form the substrate mainframe 15 separately.
[0167] When forming salients 18A and 18B in one with the substrate mainframe 15, salients 18A and 18B consist of the same quality of the material (for example, glass epoxy) as the substrate mainframe 15. Moreover, when forming salients 18A and 18B separately [the substrate mainframe 15], salients 18A and 18B can consist of a metal and insulators, such as a resin.
[0168] Drawing 48 shows the side elevation of BGA package mounted in the printed circuit board of the drawing 46 and the drawing 47 . Moreover, drawing 49 shows the bottom plan view of BGA package of drawing 48 .
[0169] This BGA package has the package mainframe (wiring substrate) 11, LSI chip 13 which was carried in this package mainframe 11 and covered by the resin 12, and two or more solder balls 14 arranged at the whole surface side of the package mainframe 11. Two or more solder balls 14 are arranged in the shape of an array at the whole surface side of the package mainframe 11.
[0170] Drawing 50 shows the side elevation of the status that BGA package of the drawing 48 and the drawing 49 was carried in the printed circuit board of the drawing 46 and drawing 47 **.

[0171] That is, since it supports to the salients 18A and 18B prepared in the printed circuit board, the crushing condition of the solder ball 14 becomes always fixed, and BGA package does not have the situation where the solder ball 14 is crushed too much.
[0172] According to the above-mentioned configuration, the linear salients 18A and 18B are formed in the whole surface side (side in which the electrode in contact with a solder ball is formed) of a printed circuit board. For this reason, these salients 18A and 18B support, and the situation where a next door and the solder ball 14 of BGA package are crushed too much is lost. Therefore, solder balls contact, the package yield does not fall and a low manufacturing cost can be attained.
[0173] Moreover, if salients 18A and 18B are constituted from a material which has low thermal resistance, a printed circuit board can also be made to emit the heat which occurs from LSI chip 13.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The side elevation showing BGA package concerning the 1st example of this invention.
[Drawing 2] The bottom plan view of BGA package of drawing 1 .
[Drawing 3] The side elevation showing the printed circuit board which carries BGA package of drawing 1 .
[Drawing 4] The plan of the printed circuit board of drawing 3 .
[Drawing 5] The side elevation showing the status that the package of drawing 1 was carried in the substrate of drawing 3 .
[Drawing 6] The side elevation showing the printed circuit board concerning the 1st example of this invention.
[Drawing 7] The plan of the printed circuit board of drawing 6 .
[Drawing 8] The side elevation showing BGA package carried in the printed circuit board of drawing 6 .
[Drawing 9] The bottom plan view of BGA package of drawing 8 .
[Drawing 10] The side elevation showing the status that the package of drawing 8 was carried in the substrate of drawing 6 .
[Drawing 11] The side elevation showing BGA package concerning the 2nd example of this invention.
[Drawing 12] The bottom plan view of BGA package of drawing 11 .
[Drawing 13] The side elevation showing the printed circuit board which carries BGA package of drawing 11 .
[Drawing 14] The plan of the printed circuit board of drawing 13 .
[Drawing 15] The side elevation showing the status that the package of drawing 11 was carried in the substrate of drawing 13 .

[Drawing 16] The side elevation showing the printed circuit board concerning the 2nd example of this invention.
[Drawing 17] The plan of the printed circuit board of drawing 16 .
[Drawing 18] The side elevation showing BGA package carried in the printed circuit board of drawing 16 .
[Drawing 19] The bottom plan view of BGA package of drawing 18 .
[Drawing 20] The side elevation showing the status that the package of drawing 18 was carried in the substrate of drawing 16 .

[Drawing 21] The side elevation showing BGA package concerning the 3rd example of this invention.
[Drawing 22] The bottom plan view of BGA package of drawing 21 .
[Drawing 23] The side elevation showing the printed circuit board concerning the 3rd example of this invention.
[Drawing 24] The plan of the printed circuit board of drawing 23 .
[Drawing 25] The side elevation showing the status that the package of drawing 21 was carried in the substrate of drawing 23 .

[Drawing 26] The side elevation showing BGA package concerning the 4th example of this invention.
[Drawing 27] The bottom plan view of BGA package of drawing 26 .
[Drawing 28] The side elevation showing the printed circuit board concerning the 4th example of this invention.
[Drawing 29] The plan of the printed circuit board of drawing 28 .
[Drawing 30] The side elevation showing the status that the package of drawing 26 was carried in the substrate of drawing 28 .

[Drawing 31] The side elevation showing BGA package concerning the 5th example of this invention.
[Drawing 32] The bottom plan view of BGA package of drawing 31 .
[Drawing 33] The side elevation showing the printed circuit board which carries BGA package of drawing 31 .
[Drawing 34] The plan of the printed circuit board of drawing 33 .
[Drawing 35] The side elevation showing the status that the package of drawing 31 was carried in the substrate of drawing 33 .

[Drawing 36] The side elevation showing the printed circuit board concerning the 5th example of this invention.
[Drawing 37] The plan of the printed circuit board of drawing 36 .
[Drawing 38] The side elevation showing BGA package carried in the printed circuit board of drawing 36 .
[Drawing 39] The bottom plan view of BGA package of drawing 38 .
[Drawing 40] The side elevation showing the status that the package of drawing 38 was carried in the substrate of drawing 36 .

[Drawing 41] The side elevation showing BGA package concerning the 6th example of this invention.
[Drawing 42] The bottom plan view of BGA package of drawing 41 .
[Drawing 43] The side elevation showing the printed circuit board which carries BGA package of drawing 41 .
[Drawing 44] The plan of the printed circuit board of drawing 43 .
[Drawing 45] The side elevation showing the status that the package of drawing 41 was carried in the substrate of drawing 43 .

[Drawing 46] The side elevation showing the printed circuit board concerning the 6th example of this invention.
[Drawing 47] The plan of the printed circuit board of drawing 46 .
[Drawing 48] The side elevation showing BGA package carried in the printed circuit board of drawing 46 .
[Drawing 49] The bottom plan view of BGA package of drawing 48 .

[Drawing 50] The side elevation showing the status that the package of drawing 48 was carried in the substrate of drawing 46

[Drawing 51] The side elevation showing the status that the conventional BGA package was carried in the printed circuit board.

[Description of Notations]
11 -- Package Mainframe (Wiring Substrate),
12 -- Resin,
13 -- LSI Chip,
14 -- Spherical Solder (Solder Ball),
15 -- Substrate Mainframe,
16 -- Electrode (Terminal),
17, 17A,-17D -- Salient of BGA package,
18, 18A,-18D -- Salient of a printed circuit board.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The side elevation showing BGA package concerning the 1st example of this invention.
[Drawing 2] The bottom plan view of BGA package of drawing 1 .
[Drawing 3] The side elevation showing the printed circuit board which carries BGA package of drawing 1 .
[Drawing 4] The plan of the printed circuit board of drawing 3 .
[Drawing 5] The side elevation showing the status that the package of drawing 1 was carried in the substrate of drawing 3 .
[Drawing 6] The side elevation showing the printed circuit board concerning the 1st example of this invention.
[Drawing 7] The plan of the printed circuit board of drawing 6 .
[Drawing 8] The side elevation showing BGA package carried in the printed circuit board of drawing 6 .
[Drawing 9] The bottom plan view of BGA package of drawing 8 .
[Drawing 10] The side elevation showing the status that the package of drawing 8 was carried in the substrate of drawing 6 .
[Drawing 11] The side elevation showing BGA package concerning the 2nd example of this invention.
[Drawing 12] The bottom plan view of BGA package of drawing 11 .
[Drawing 13] The side elevation showing the printed circuit board which carries BGA package of drawing 11 .
[Drawing 14] The plan of the printed circuit board of drawing 13 .
[Drawing 15] The side elevation showing the status that the package of drawing 11 was carried in the substrate of drawing 13 .

[Drawing 16] The side elevation showing the printed circuit board concerning the 2nd example of this invention.
[Drawing 17] The plan of the printed circuit board of drawing 16 .
[Drawing 18] The side elevation showing BGA package carried in the printed circuit board of drawing 16 .
[Drawing 19] The bottom plan view of BGA package of drawing 18 .
[Drawing 20] The side elevation showing the status that the package of drawing 18 was carried in the substrate of drawing 16 .

[Drawing 21] The side elevation showing BGA package concerning the 3rd example of this invention.
[Drawing 22] The bottom plan view of BGA package of drawing 21 .
[Drawing 23] The side elevation showing the printed circuit board concerning the 3rd example of this invention.
[Drawing 24] The plan of the printed circuit board of drawing 23 .
[Drawing 25] The side elevation showing the status that the package of drawing 21 was carried in the substrate of drawing 23 .

[Drawing 26] The side elevation showing BGA package concerning the 4th example of this invention.
[Drawing 27] The bottom plan view of BGA package of drawing 26 .
[Drawing 28] The side elevation showing the printed circuit board concerning the 4th example of this invention.
[Drawing 29] The plan of the printed circuit board of drawing 28 .
[Drawing 30] The side elevation showing the status that the package of drawing 26 was carried in the substrate of drawing 28 .

[Drawing 31] The side elevation showing BGA package concerning the 5th example of this invention.
[Drawing 32] The bottom plan view of BGA package of drawing 31 .
[Drawing 33] The side elevation showing the printed circuit board which carries BGA package of drawing 31 .
[Drawing 34] The plan of the printed circuit board of drawing 33 .
[Drawing 35] The side elevation showing the status that the package of drawing 31 was carried in the substrate of drawing 33 .

[Drawing 36] The side elevation showing the printed circuit board concerning the 5th example of this invention.
[Drawing 37] The plan of the printed circuit board of drawing 36 .
[Drawing 38] The side elevation showing BGA package carried in the printed circuit board of drawing 36 .
[Drawing 39] The bottom plan view of BGA package of drawing 38 .
[Drawing 40] The side elevation showing the status that the package of drawing 38 was carried in the substrate of drawing 36 .

[Drawing 41] The side elevation showing BGA package concerning the 6th example of this invention.
[Drawing 42] The bottom plan view of BGA package of drawing 41 .
[Drawing 43] The side elevation showing the printed circuit board which carries BGA package of drawing 41 .
[Drawing 44] The plan of the printed circuit board of drawing 43 .
[Drawing 45] The side elevation showing the status that the package of drawing 41 was carried in the substrate of drawing 43 .

[Drawing 46] The side elevation showing the printed circuit board concerning the 6th example of this invention.
[Drawing 47] The plan of the printed circuit board of drawing 46 .
[Drawing 48] The side elevation showing BGA package carried in the printed circuit board of drawing 46 .
[Drawing 49] The bottom plan view of BGA package of drawing 48 .

[Drawing 50] The side elevation showing the status that the package of drawing 48 was carried in the substrate of drawing 46.

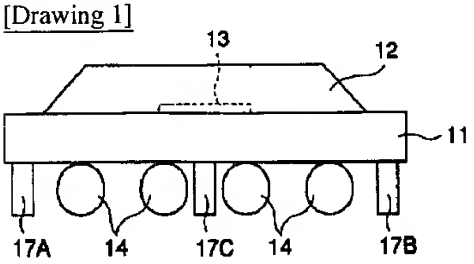
[Drawing 51] The side elevation showing the status that the conventional BGA package was carried in the printed circuit board.

[Description of Notations]
11 -- Package Mainframe (Wiring Substrate),
12 -- Resin,
13 -- LSI Chip,
14 -- Spherical Solder (Solder Ball),
15 -- Substrate Mainframe,
16 -- Electrode (Terminal),
17, 17A,-17D -- Salient of BGA package,
18, 18A,-18D -- Salient of a printed circuit board.

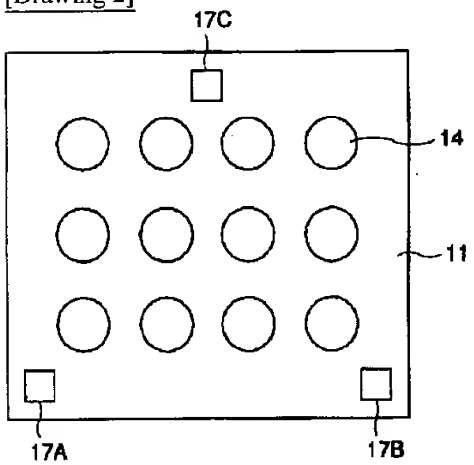
[Translation done.]

DRAWINGS

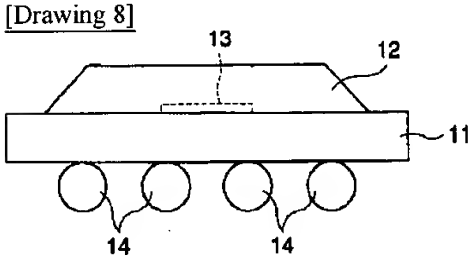
[Drawing 1]



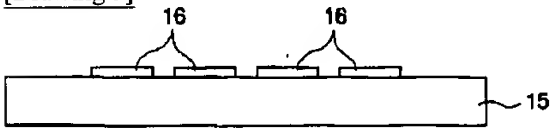
[Drawing 2]



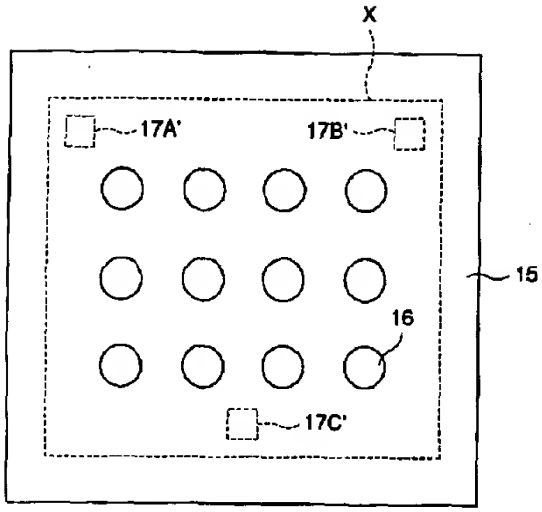
[Drawing 8]



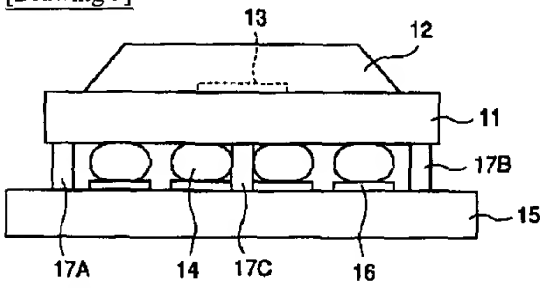
[Drawing 3]



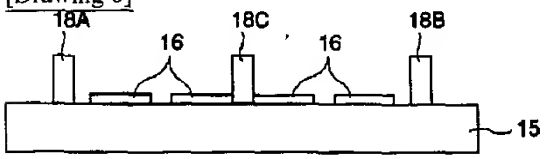
[Drawing 4]



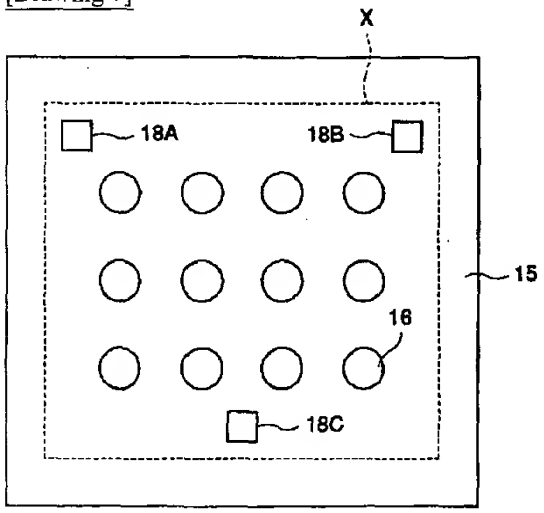
[Drawing 5]



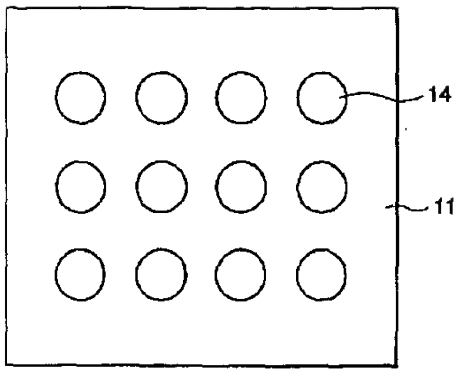
[Drawing 6]



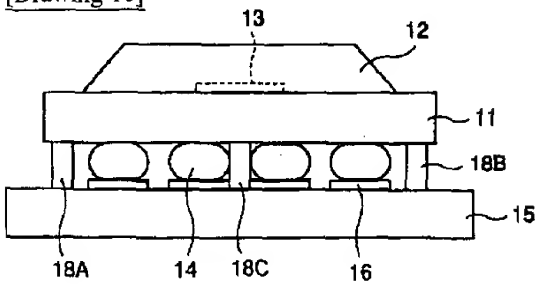
[Drawing 7]



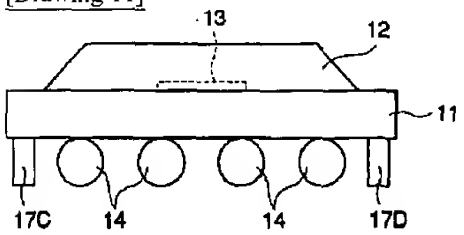
[Drawing 9]



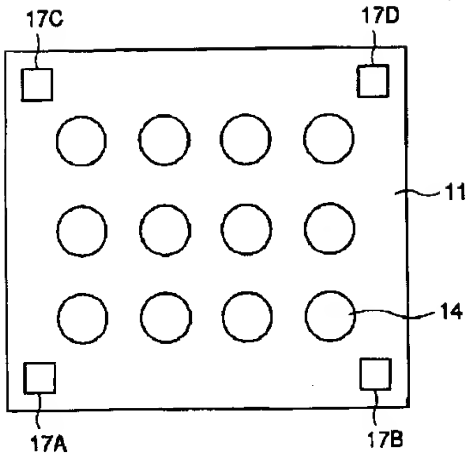
[Drawing 10]



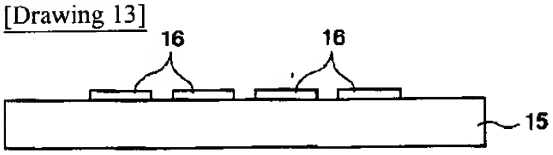
[Drawing 11]



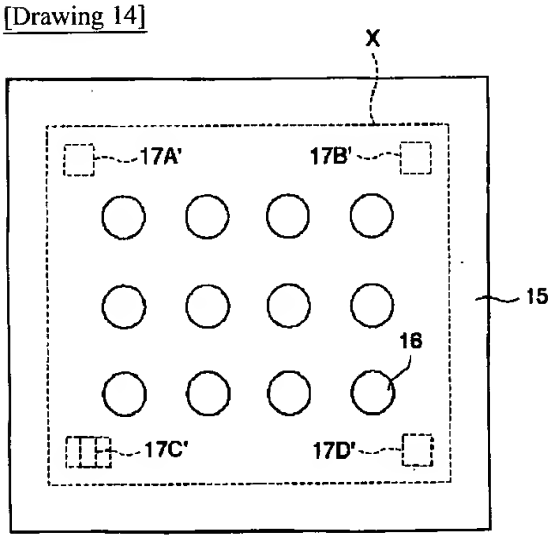
[Drawing 12]



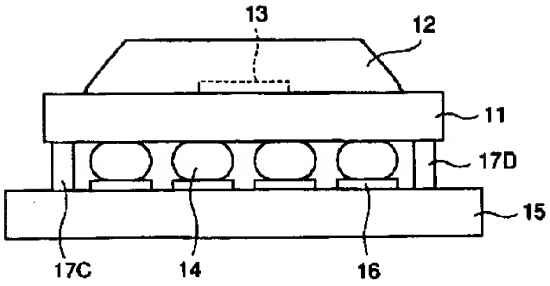
[Drawing 13]



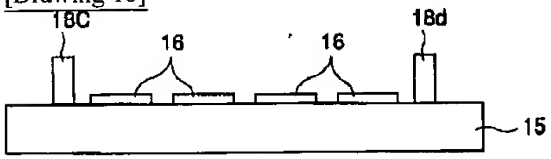
[Drawing 14]



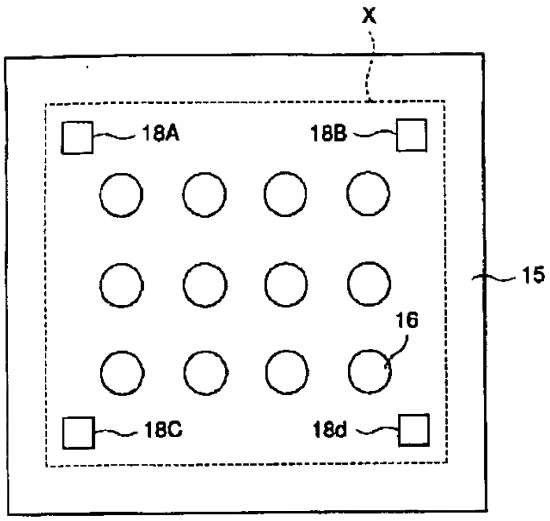
[Drawing 15]



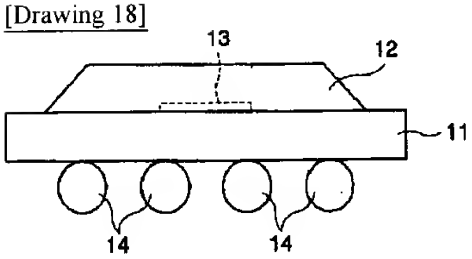
[Drawing 16]



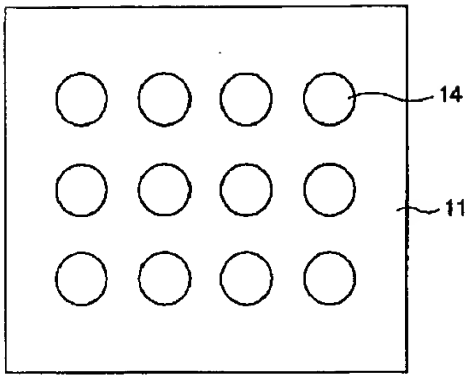
[Drawing 17]



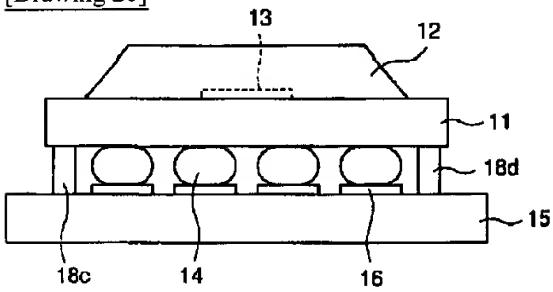
[Drawing 18]



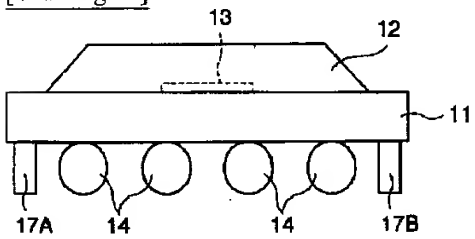
[Drawing 19]



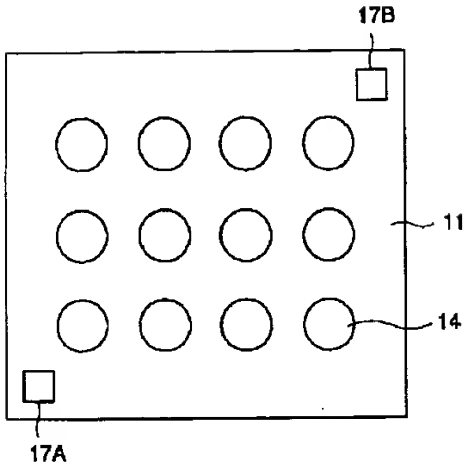
[Drawing 20]



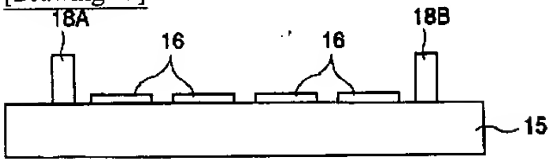
[Drawing 21]



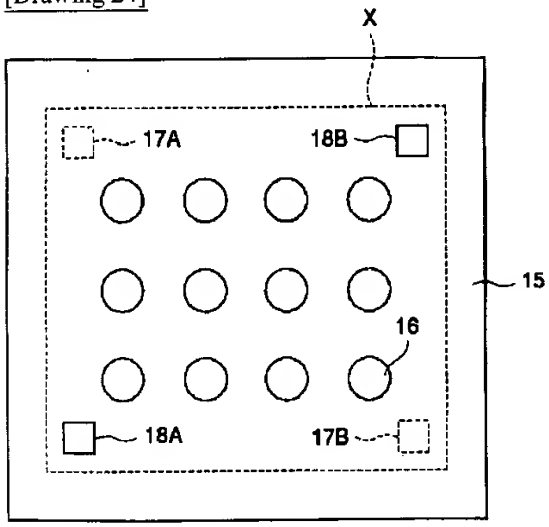
[Drawing 22]



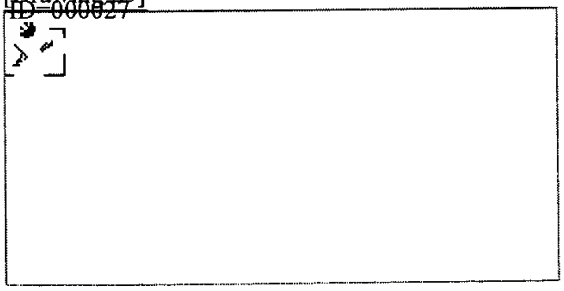
[Drawing 23]



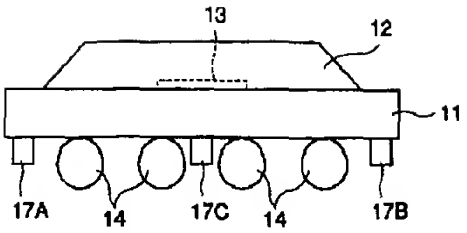
[Drawing 24]



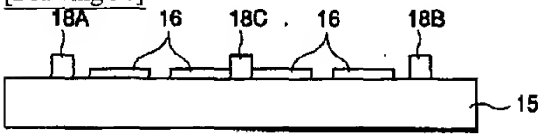
[Drawing 25]



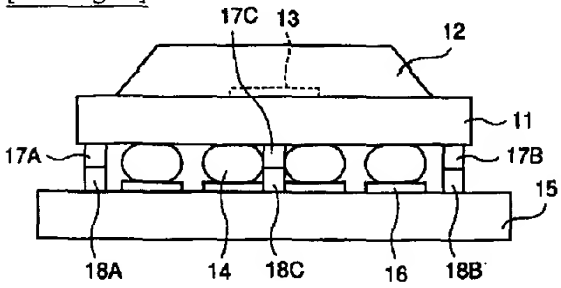
[Drawing 26]



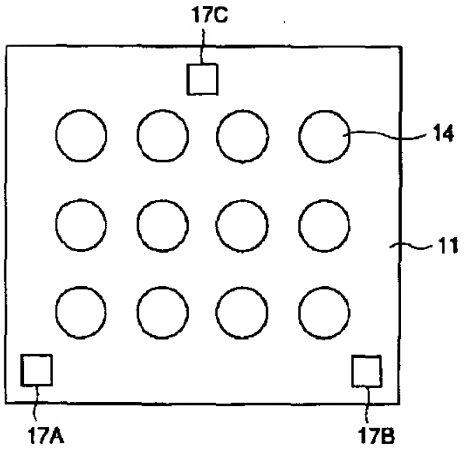
[Drawing 28]



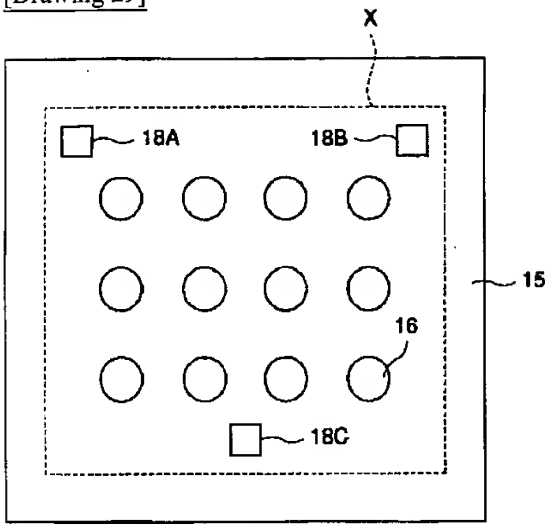
[Drawing 30]



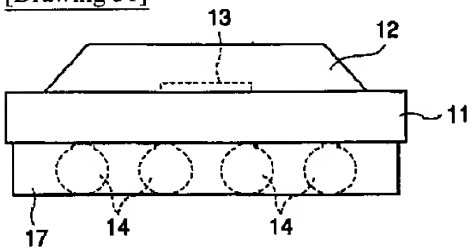
[Drawing 27]



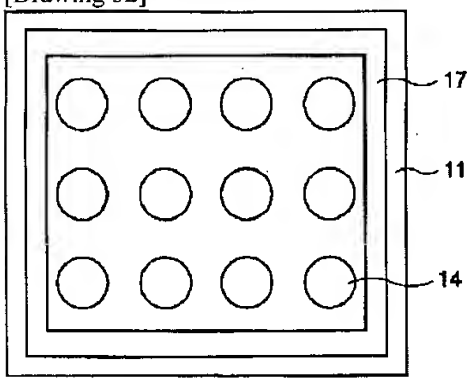
[Drawing 29]



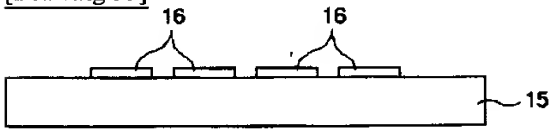
[Drawing 31]



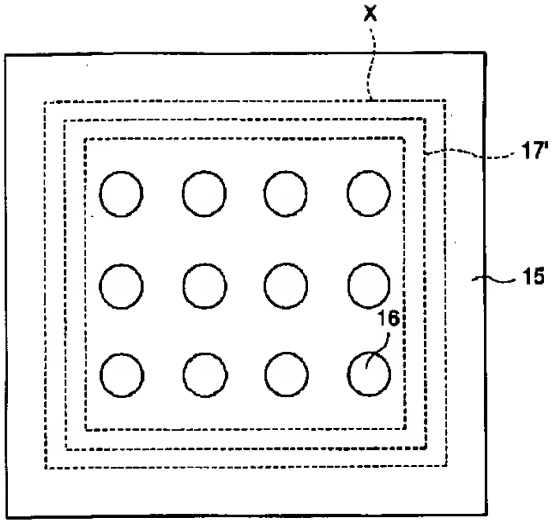
[Drawing 32]



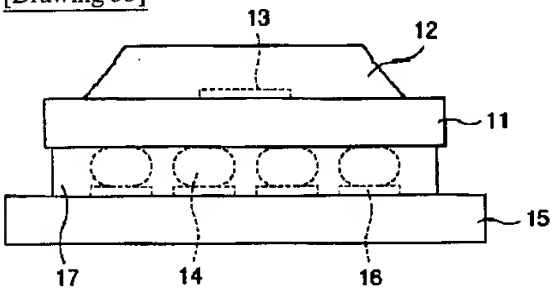
[Drawing 33]



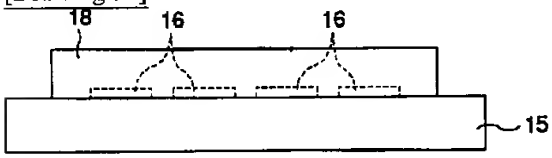
[Drawing 34]



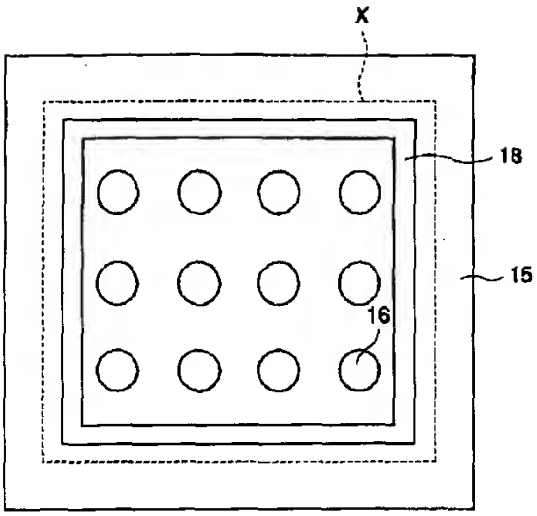
[Drawing 35]



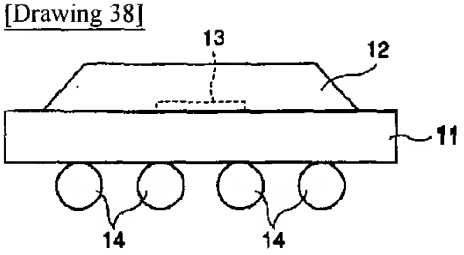
[Drawing 36]



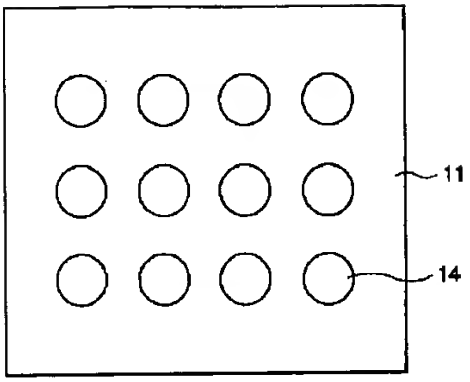
[Drawing 37]



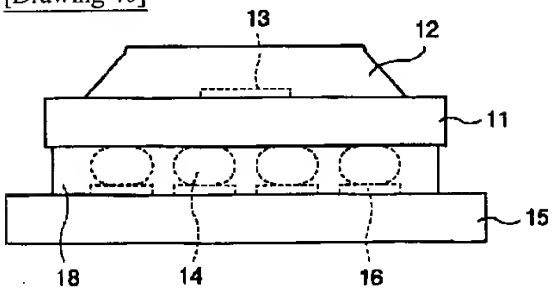
[Drawing 38]



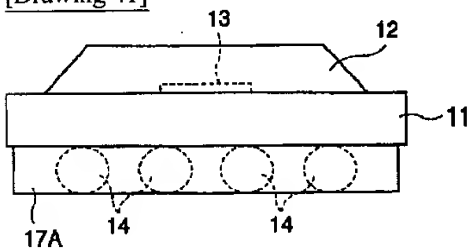
[Drawing 39]



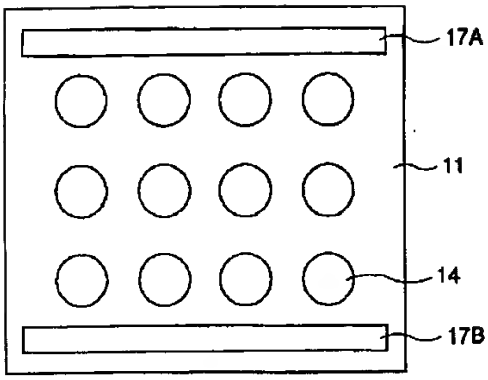
[Drawing 40]



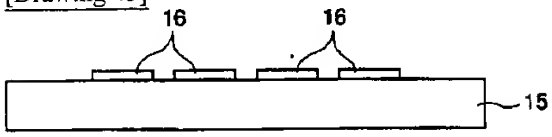
[Drawing 41]



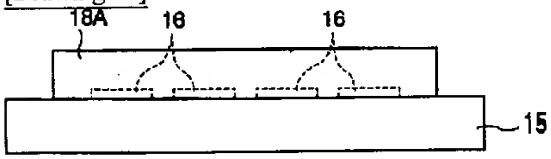
[Drawing 42]



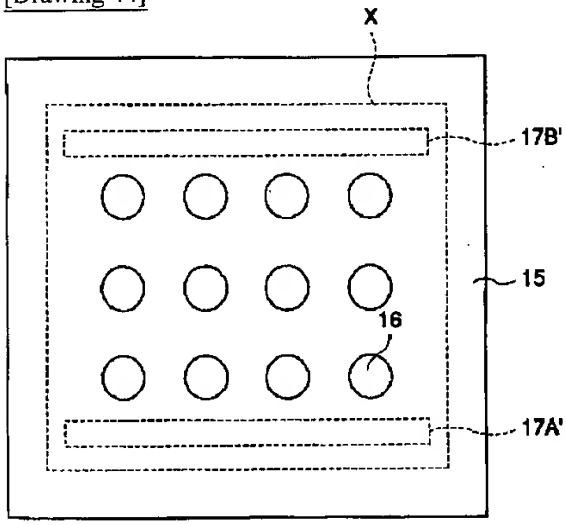
[Drawing 43]



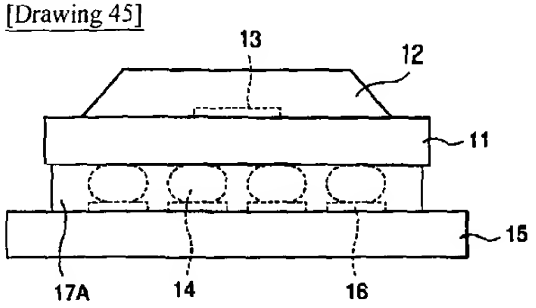
[Drawing 46]



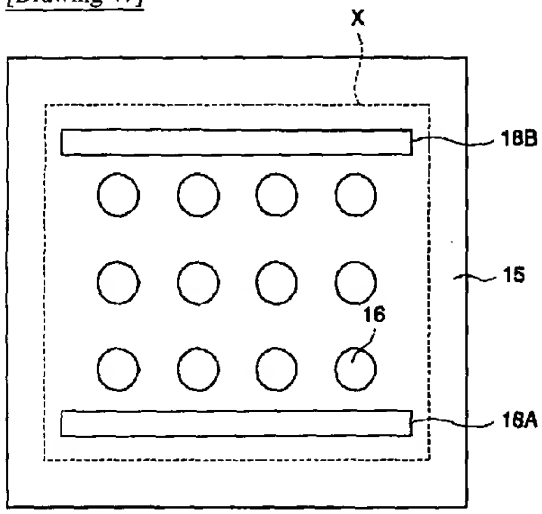
[Drawing 44]



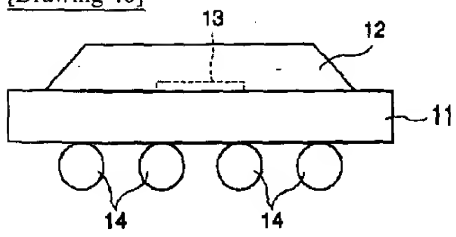
[Drawing 45]



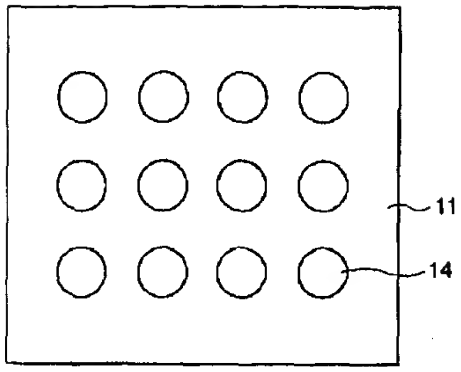
[Drawing 47]



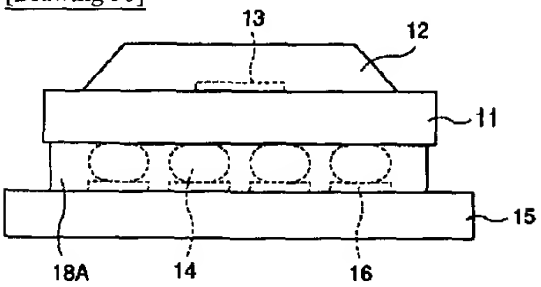
[Drawing 48]



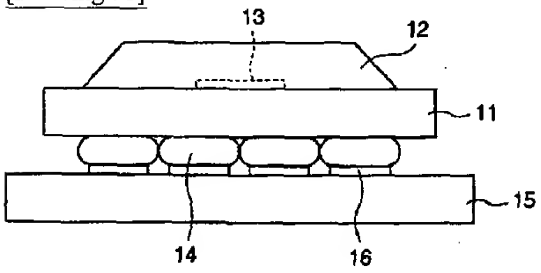
[Drawing 49]



[Drawing 50]



[Drawing 51]



[Translation done.]